

# Janus Schematic Beema

2014-03-05

REV : A00

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*DY : None Installed*

*UMA: UMA only installed*

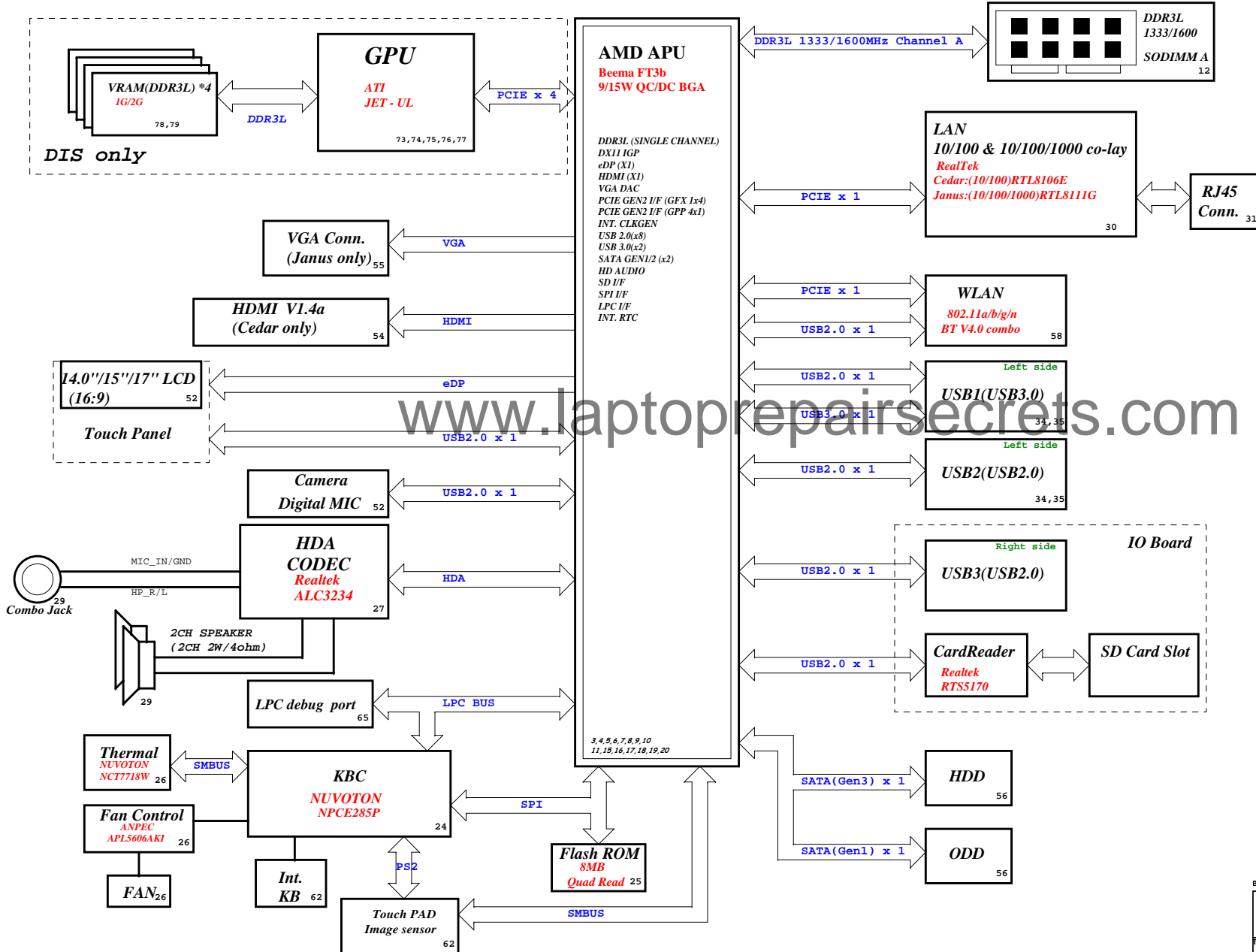
*OPS: DISCRTE SG installed*

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Title			
<b>Cover Page</b>			
Size A3	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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Project code:4PD00G010001  
PCB P/N: 13325-1  
Revision: A00

# Janus Block Diagram

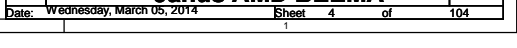
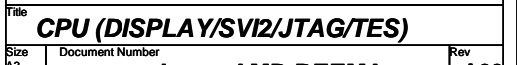
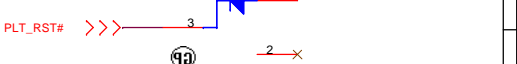
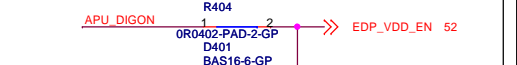
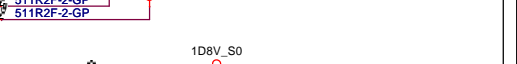
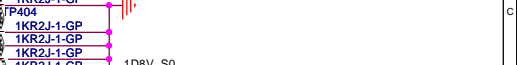
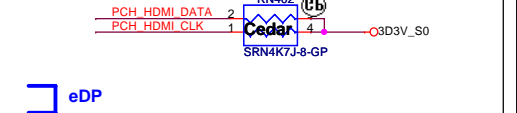
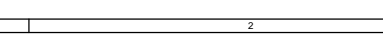
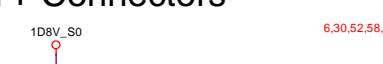
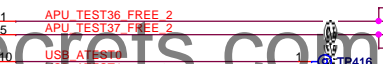
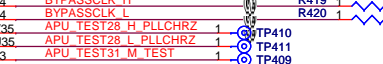
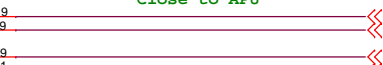
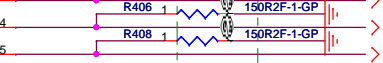
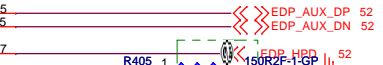
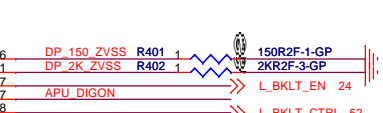
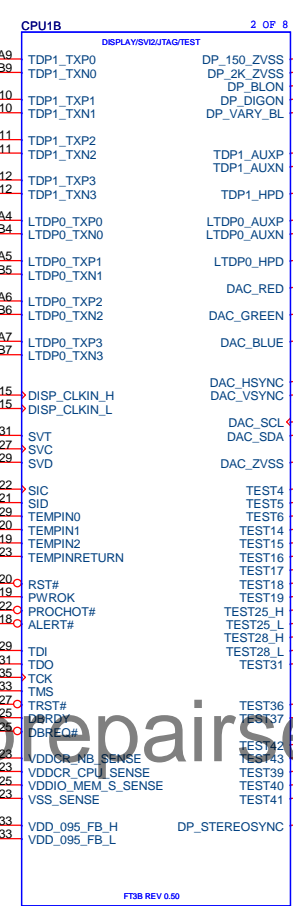
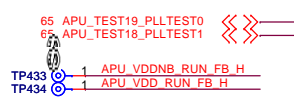
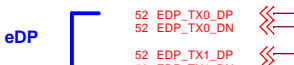
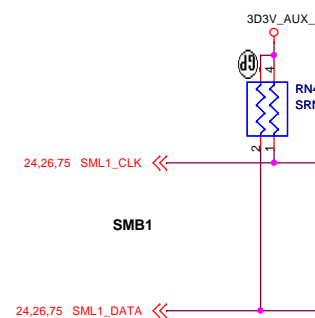
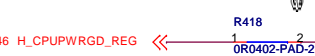
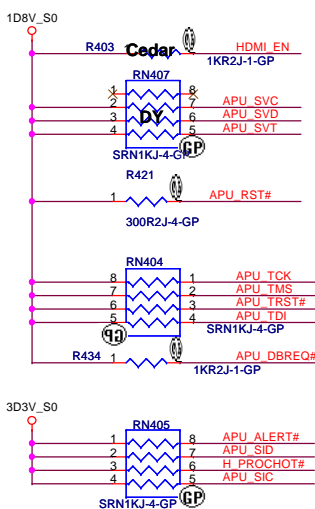


CHARGER	
BQ24727RGRR	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95813HRZ-GP	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
VDDIO_AZ	
TLV70215DBVR	36
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
36	83
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
0D95V_S5	0D95V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
1D8V_S5	1D8V_VGA_S0
PCB LAYER	
L1:TOP L2:VCC L3:Signal L4:Signal L5:GND L6:BOT	



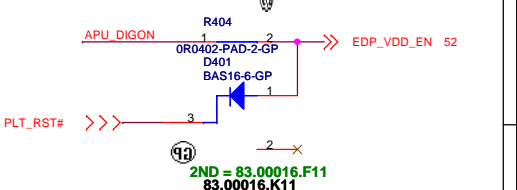
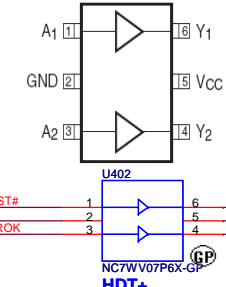
Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

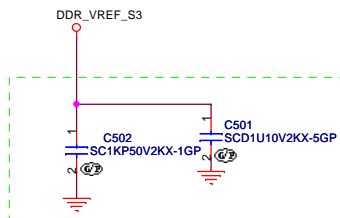
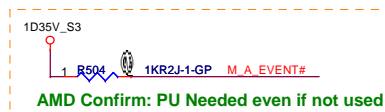


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HDT+ Connectors



Wistron Corporation logo and information. Title: CPU (DISPLAY/SVIZ/JTAG/TES). Document Number: Janus AMD BEEMA. Date: Wednesday, March 05, 2014. Sheet 4 of 104.



LAYOUT: place them close to APU

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3D3V\_S0

There are integrated pull-up.

R635 1 10KR2J-3-GP BLUETOOTH\_EN

R603 1 10KR2J-3-GP H\_A2OGATE

R604 1 10KR2J-3-GP KB\_DET#

R601 1 10KR2J-3-GP DBC\_EN

24,65 LPC\_RST# << 1 2 R602 0R0402-PAD-2-GP LPC\_RST#\_C

CEDAR_JANUS_ID	
1	CEDAR
0	JANUS

3.3V\_S5

R630 100k 10KR2J-3-GP PM\_PWRBTN# R

R634 10k 10KR2J-3-GP RTC\_DET#

R617 100k 10KR2J-3-GP AC\_PRESENT

R626 100k 100KR2J-1-GP PCIE\_WAKE# R

R629		100KR2J-1GP	PM_RSMRST#
R633		10KR2J-3GP	HDA_SDIO0
R607		10KR2J-3GP	PE_GPIO0
R620		10KR2J-3GP	GEVENT#4
R621		10KR2J-3GP	GEVENT#7
R647		15KR2J-1GP	APU_TEST0
R646		15KR2J-1GP	APU_TEST1
R645		15KR2J-1GP	APU_TEST2
R632		10KR2J-3GP	GPIO71
R644		10KR2J-3GP	MEM_1V5

[illegible]

2 2 C868  
SC10P50V2JN-1GP

39K X1

XTAL-320P68KHZ-17-GP X801

R623  
20MR3-GP

32K X2

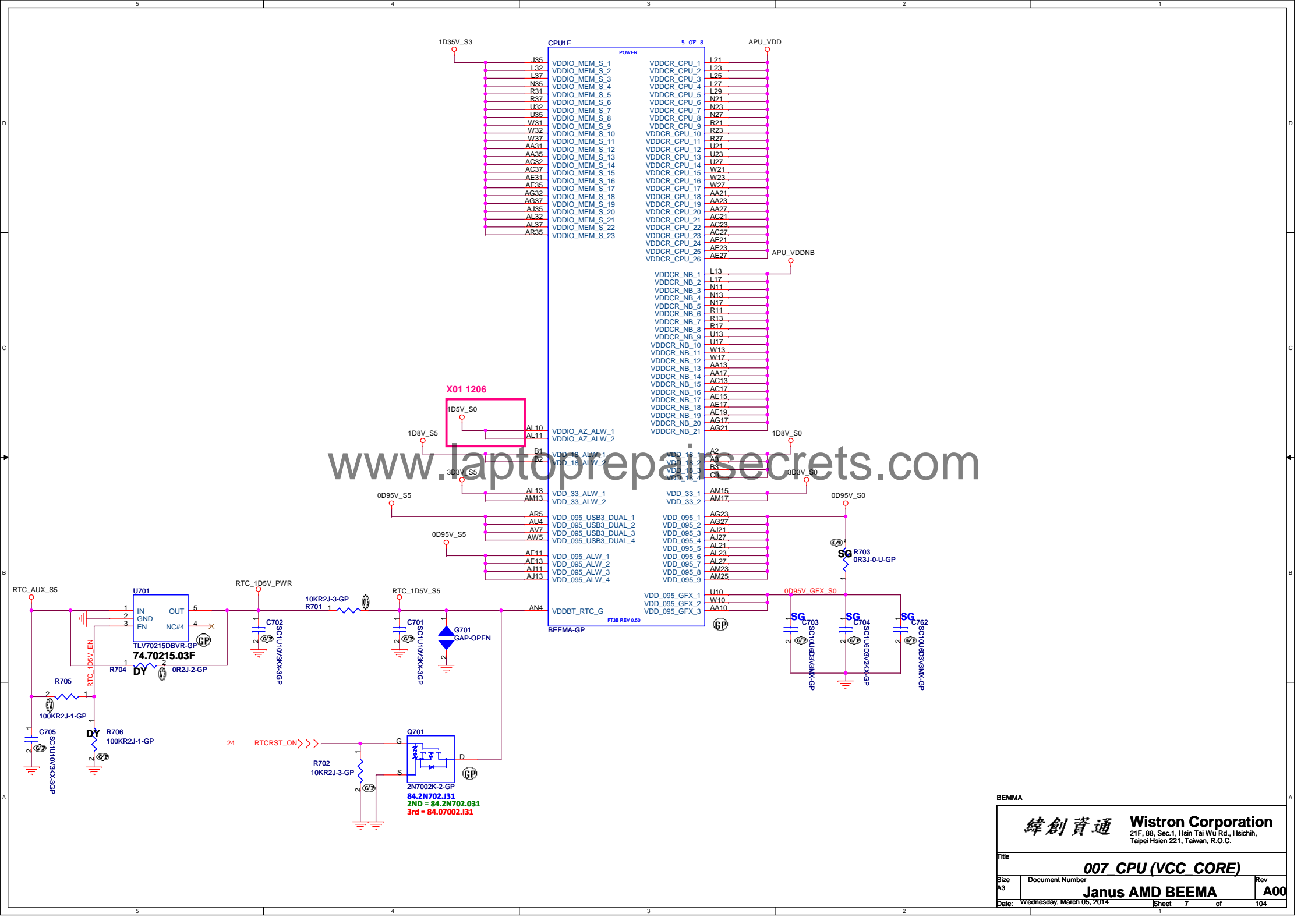
2 1 C804  
SC10P50V2JN-4GP

AMD suggests Xtal ESR must be less than 65R

	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M
3	VGA	27M

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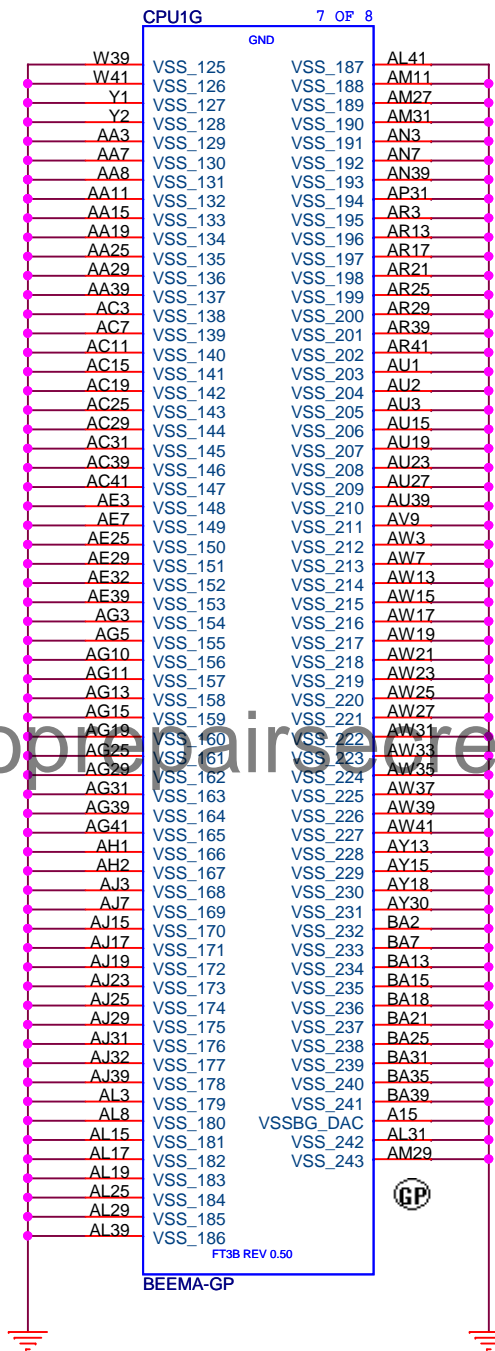
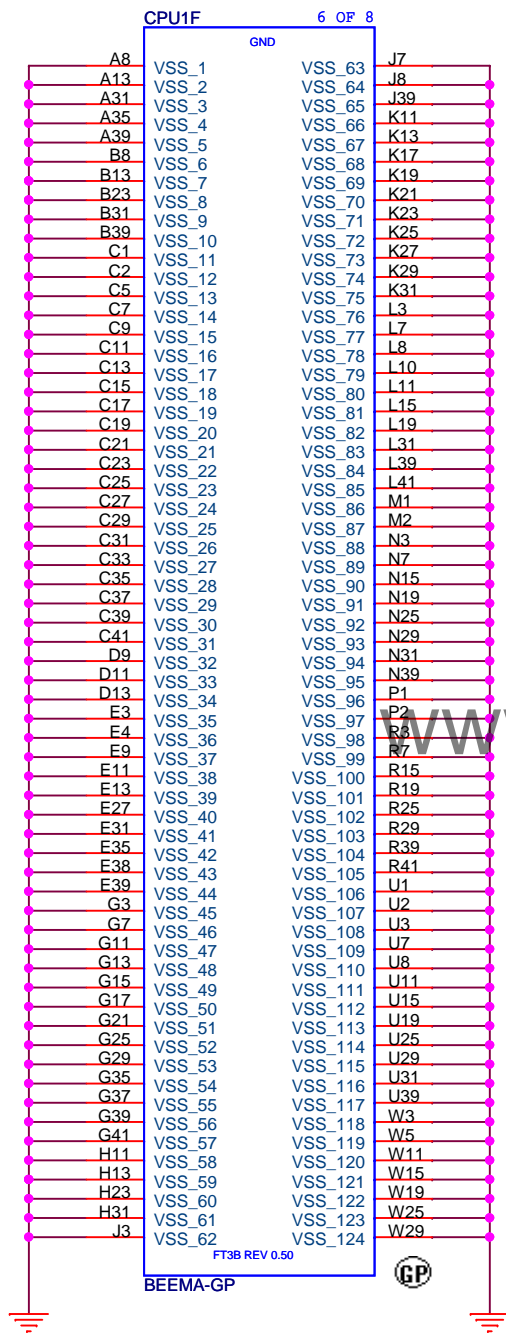
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Title

**CPU (VSS)**

Size  
A4

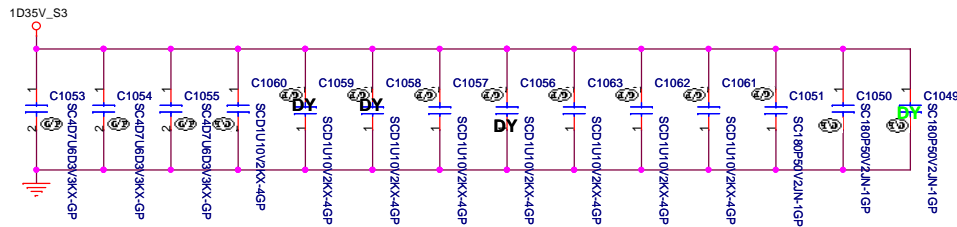
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**Janus AMD BEEMA**

Rev  
**A00**

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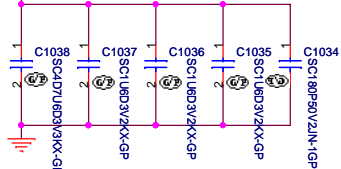
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X01 1206

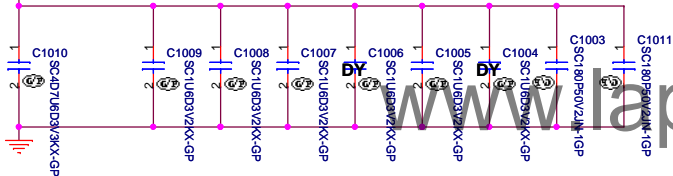
1D5V\_S0

Close to VDDIO\_AZ\_ALW



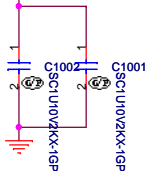
1D8V\_S5

Close to VDD\_18\_ALW

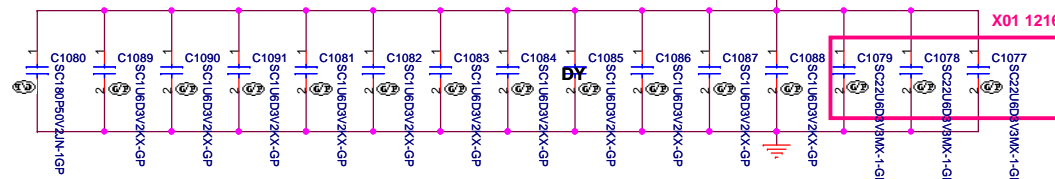
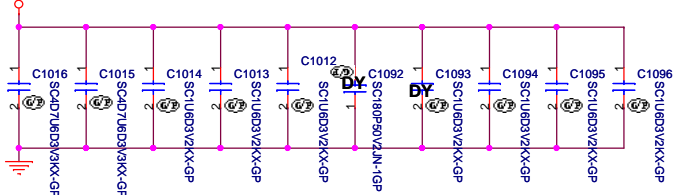


3D3V\_S5

Close to VDD\_33\_ALW

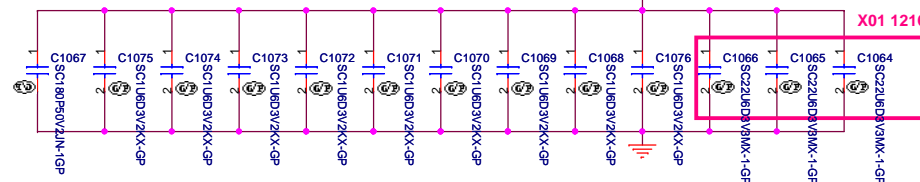


0D95V\_S5



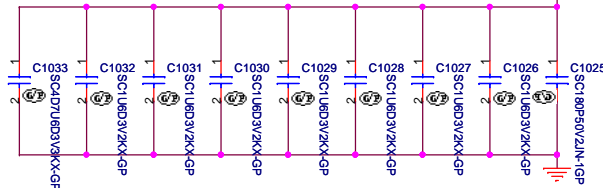
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APU\_VDDNB



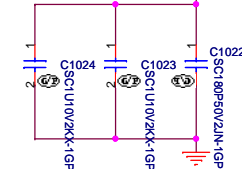
X01 1216

Close to VDD\_18



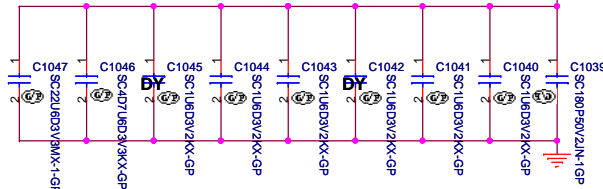
1D8V\_S0

Close to VDD\_33



3D3V\_S0

Close to VDD\_095



0D95V\_S0

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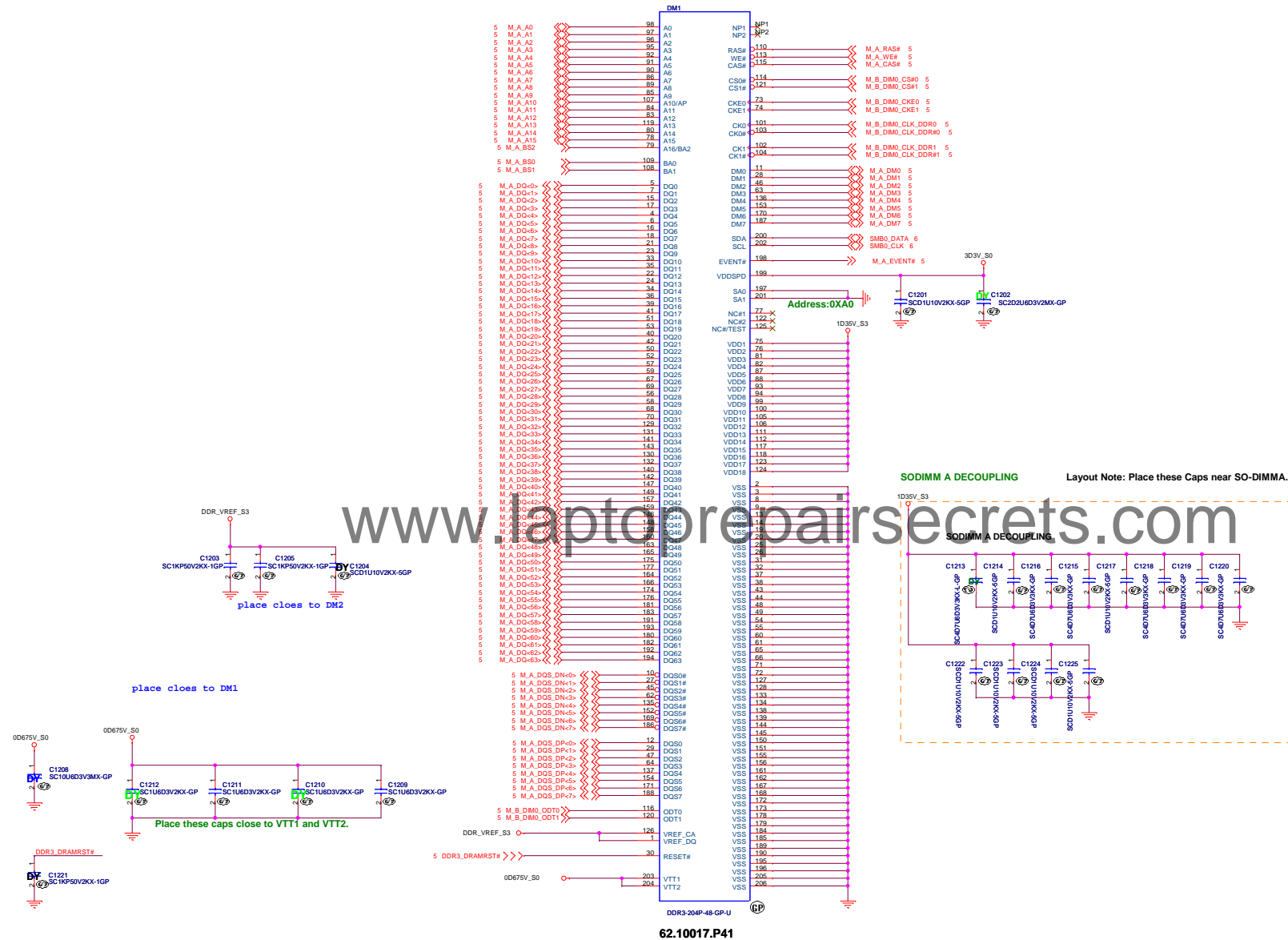
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**SSID = MEMORY**



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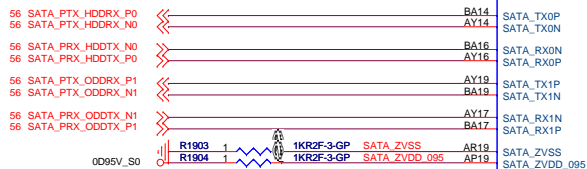
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SATA HDD

ODD

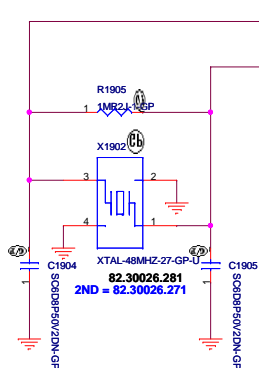
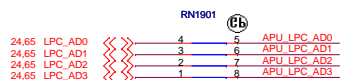
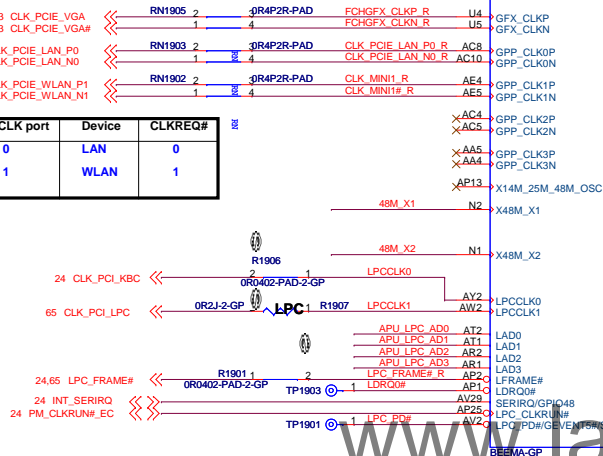


SATA	
Pair	Device
0	SATA HDD
1	ODD

LAN

WLAN

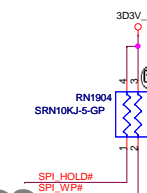
GPP CLK port	Device	CLKREQ#
0	LAN	0
1	WLAN	1



## USB Table

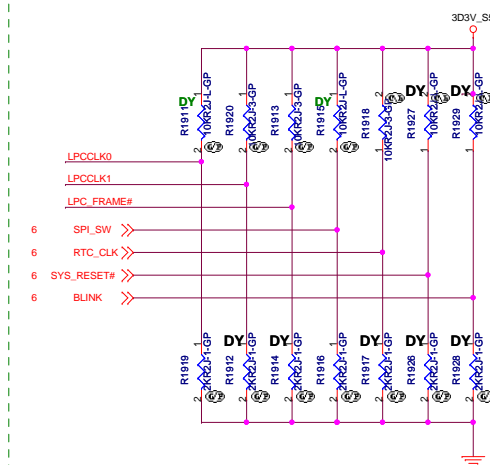
Pair	Device
0	USB2.0 PORT1 Debug
1	USB2.0 PORT3 (DB Conn)
2	
3	NA
4	Card Reader
5	WLAN + BT (Mini PCI-E)
6	Touch Panel
7	CCD (CCD Conn)
0/8	USB3.0 & USB 2.0 (MB port2)
1/9	

XTAL	CLK, Hz
0	System & USB 48M
1	RTC 32.768K
2	LAN 25M
3	VGA 27M



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## SYSTEM STRAPPINGS



## REQUIRED SYSTEM STRAPS

	LPC_CLK0	LPC_CLK1	LPC_FRAME#	SPI_SELECT	RTC_CLK	SYS_RESET#	BLINK
PULL HIGH	Boot Fail Timer Enabled	CLKGEN ENABLED	SPI ROM	1.8V SPI ROM	Coin Battery	NORMAL POWR UP /RESET TIMING	PWROK and RST_L pin routed to APU
PULL LOW	Boot Fail Timer Disabled	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM	Direct DC	Reserved	Reserved

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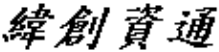
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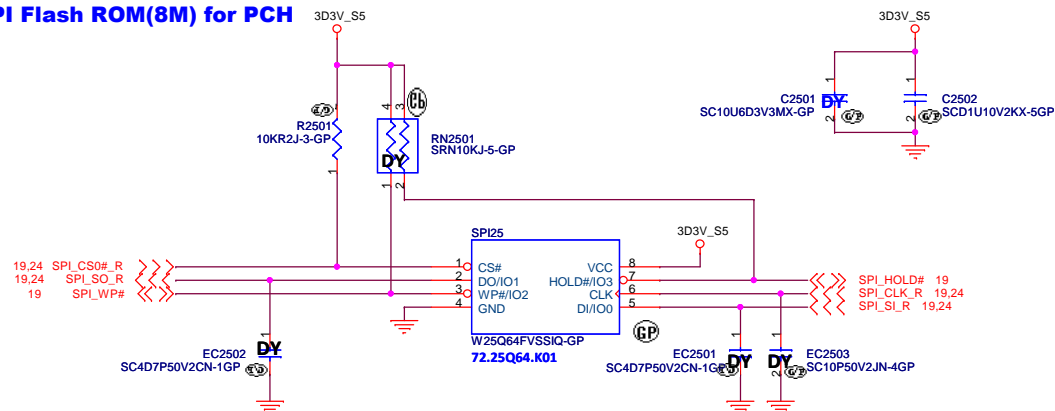
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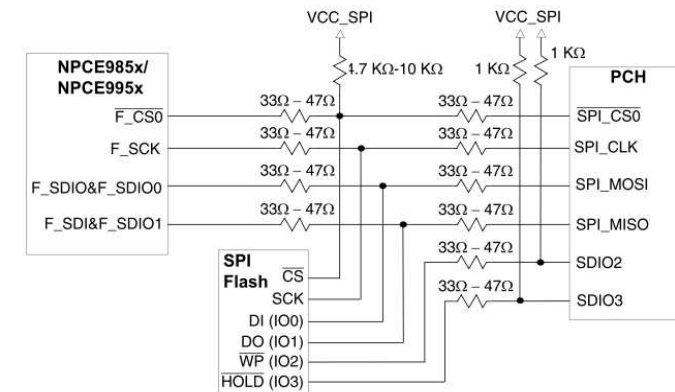
**SSID = Flash.ROM**

# SPI Flash ROM(8M) for PCH



Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

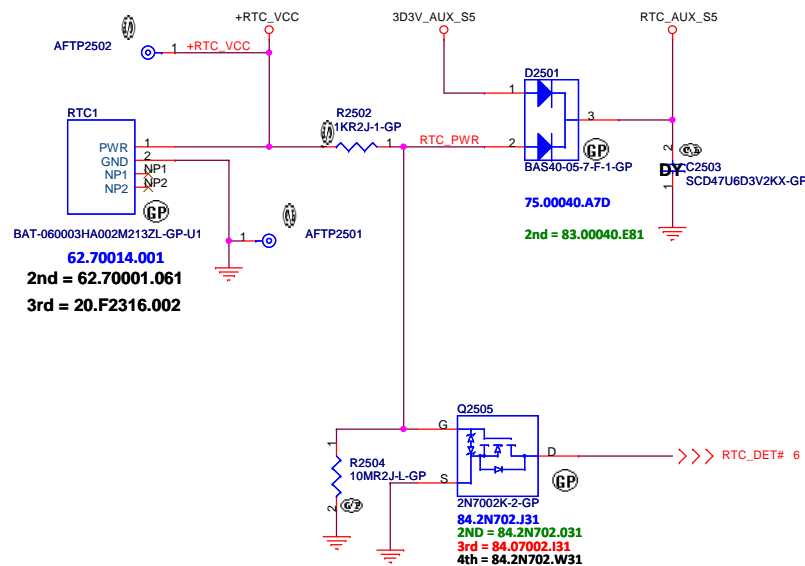
## Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

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**SSID = RBATT**

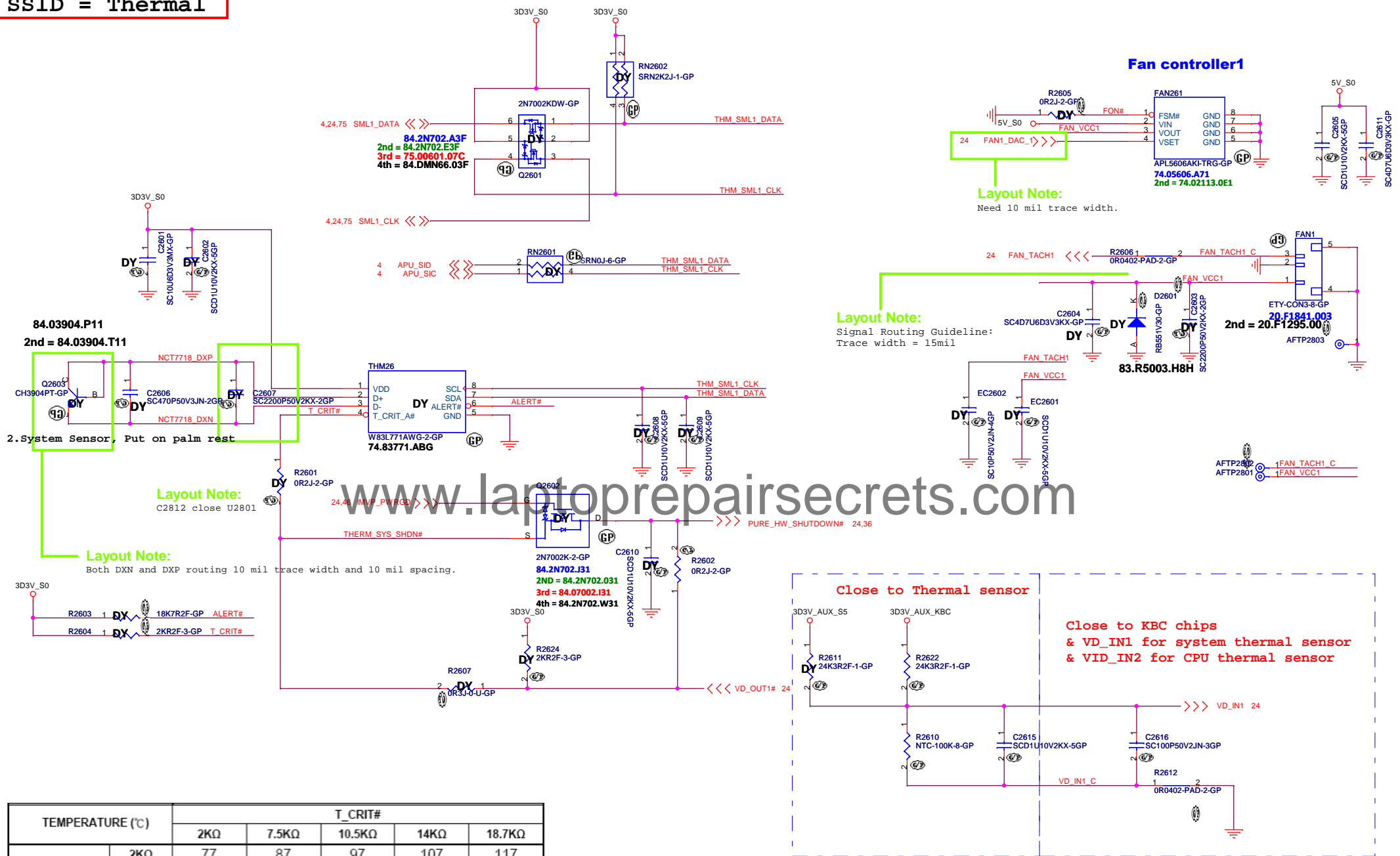


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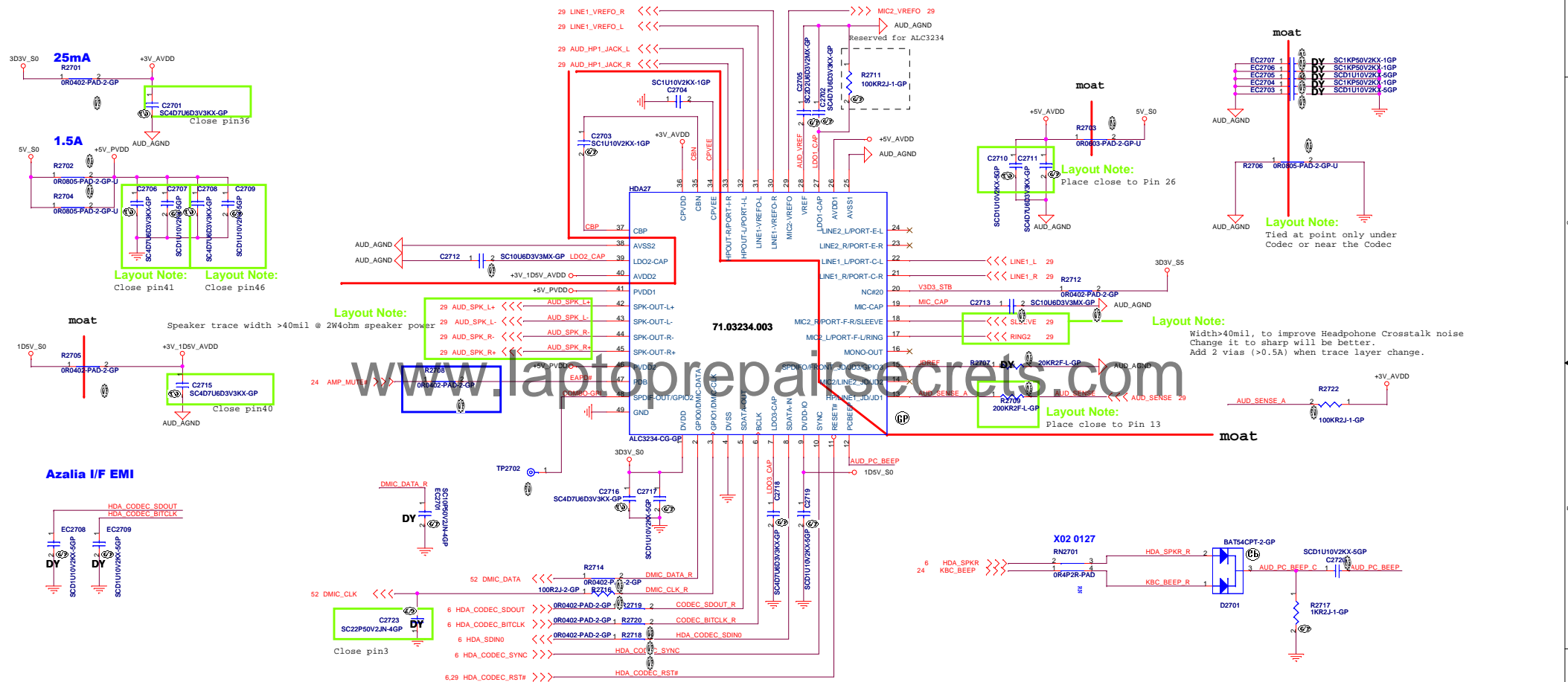
Title	Flash/RTC	
Size	Document Number	Rev
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SSID = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

SSID = AUDIO



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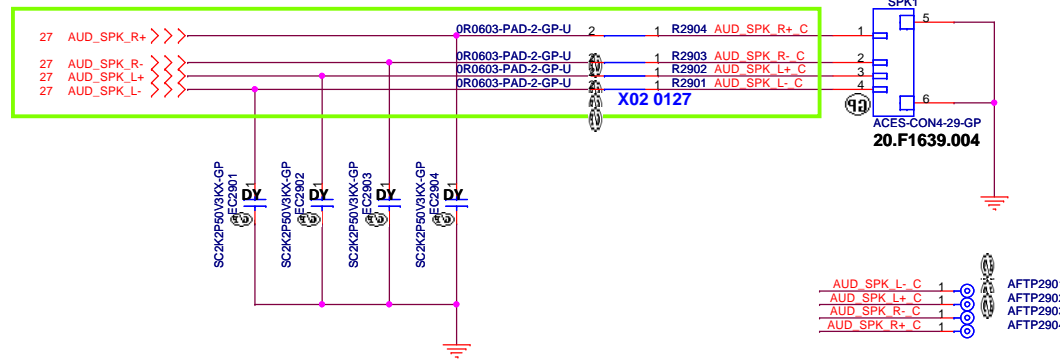
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SSID = AUDIO

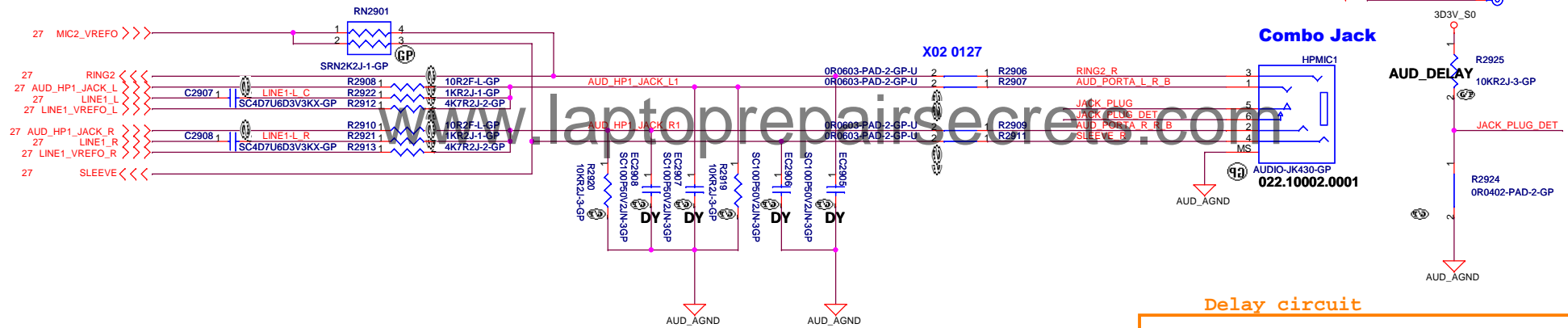
### Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

AUD\_SPK\_L- C 1 AFTP2901  
AUD\_SPK\_L+ C 1 AFTP2902  
AUD\_SPK\_R- C 1 AFTP2903  
AUD\_SPK\_R+ C 1 AFTP2904



### Combo Jack

HPMIC1

AUD\_DELAY

JACK\_PLUG

JACK\_PLUG\_DET

AUD\_DELAY

AUD\_DELAY

AUD\_DELAY

AUD\_DELAY

AUD\_DELAY

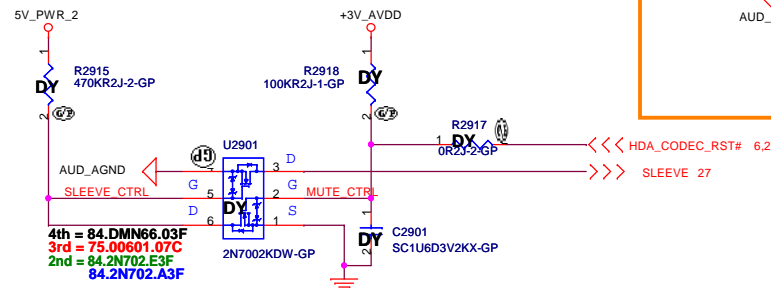
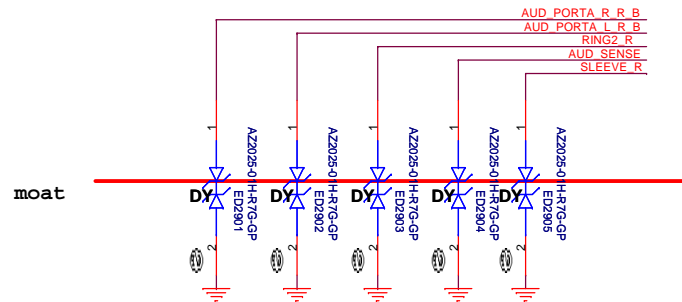
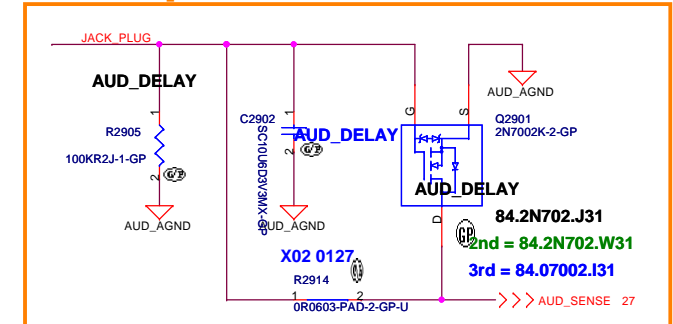
AUD\_DELAY

AUD\_DELAY

AUD\_DELAY

AUD\_DELAY

### Delay circuit

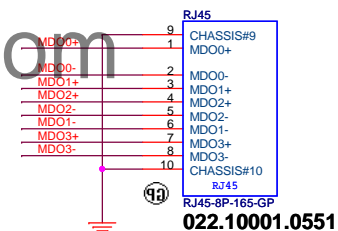
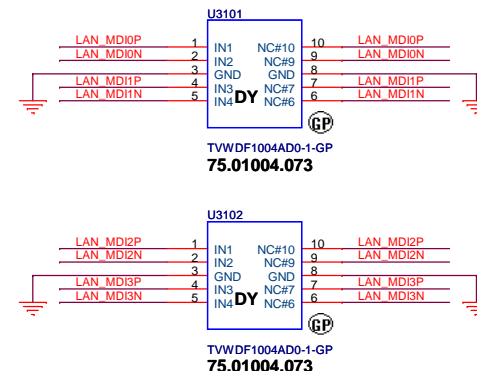
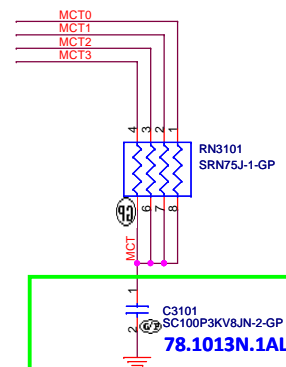
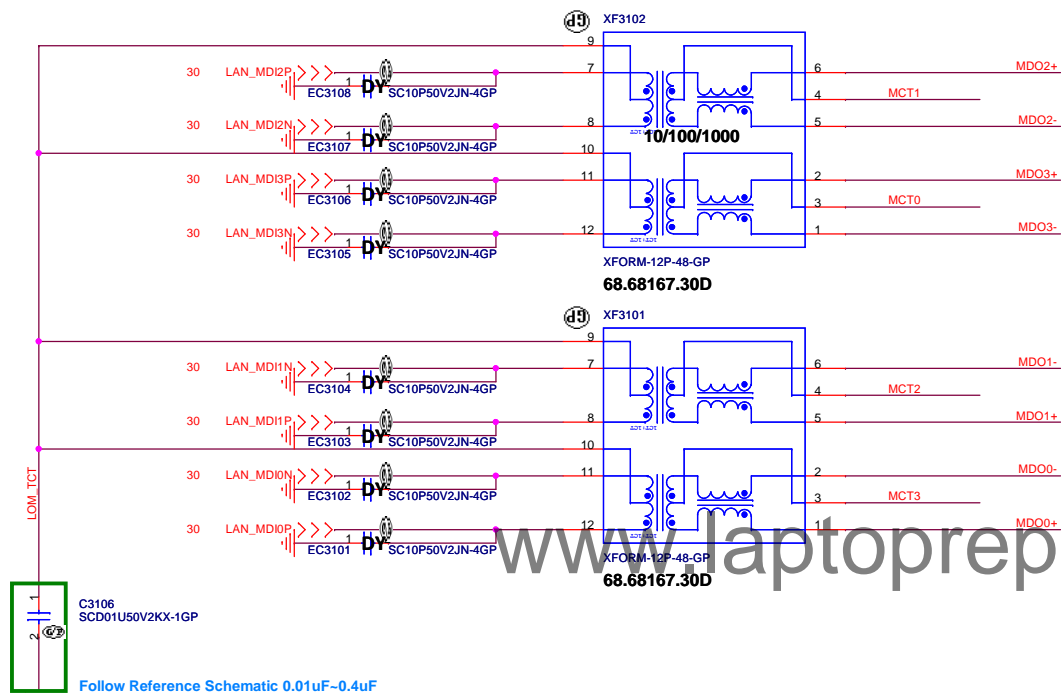




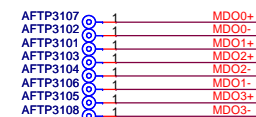
SSID = LOM

## LAN TransFormer (10/100/1000M & 10/100M co-lay)

Layout note:  
30 mil spacing between MDI differential pairs.



Layout:  
Place near RJ45



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Title		
<div>(Reserved)Card Reader</div>		
Size	Document Number	Rev
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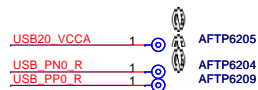
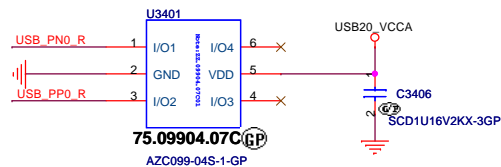
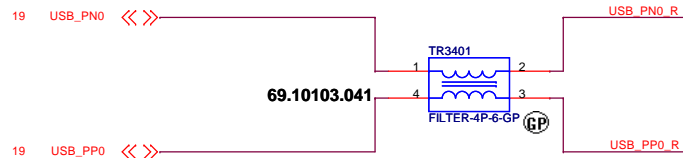
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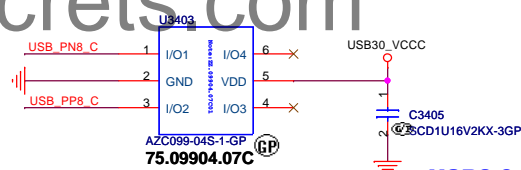
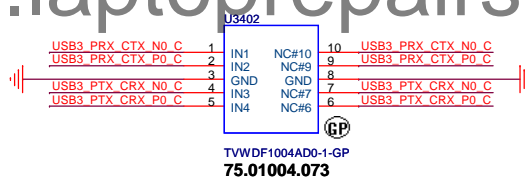
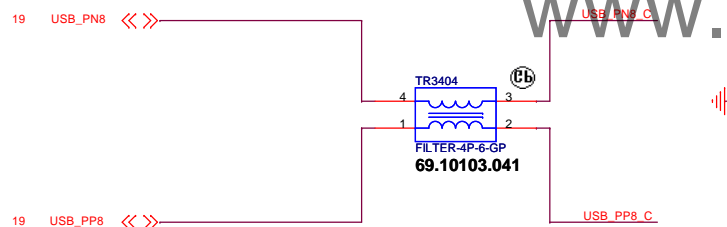
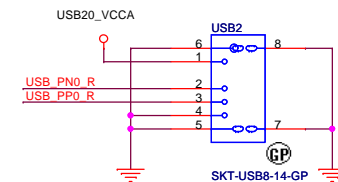
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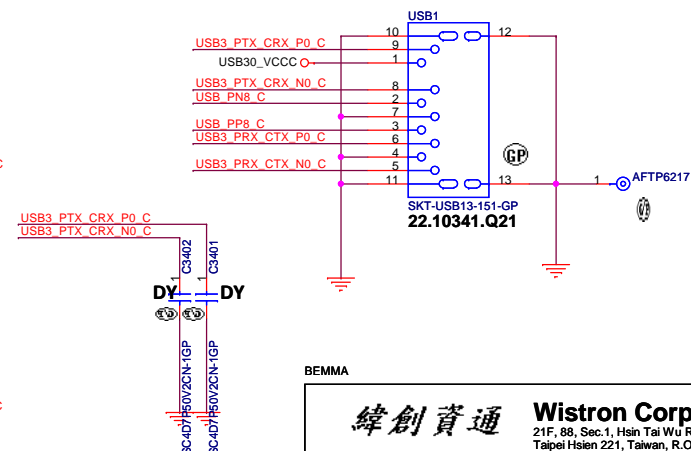
SSID = USB



## USB2.0 Port2



## USB3.0 Port1



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USB 3.0

Size

Document Number

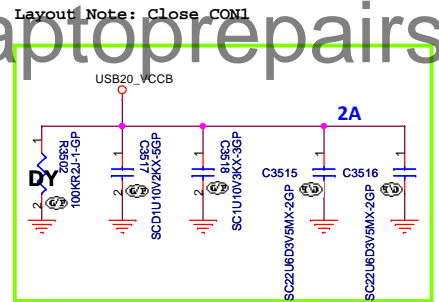
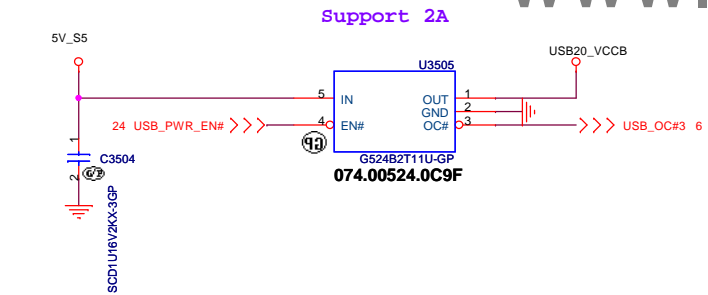
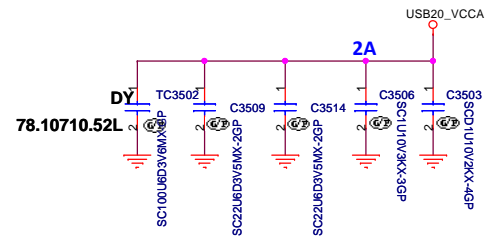
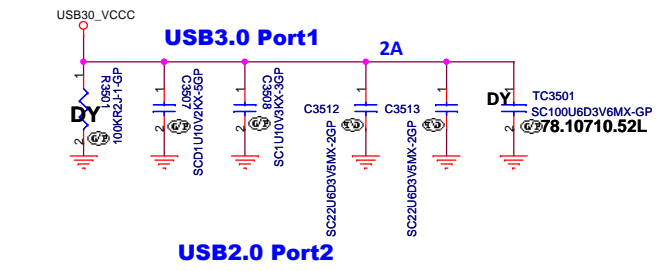
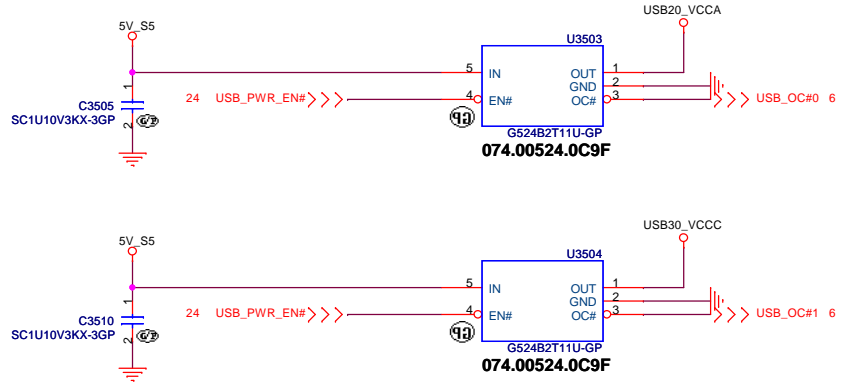
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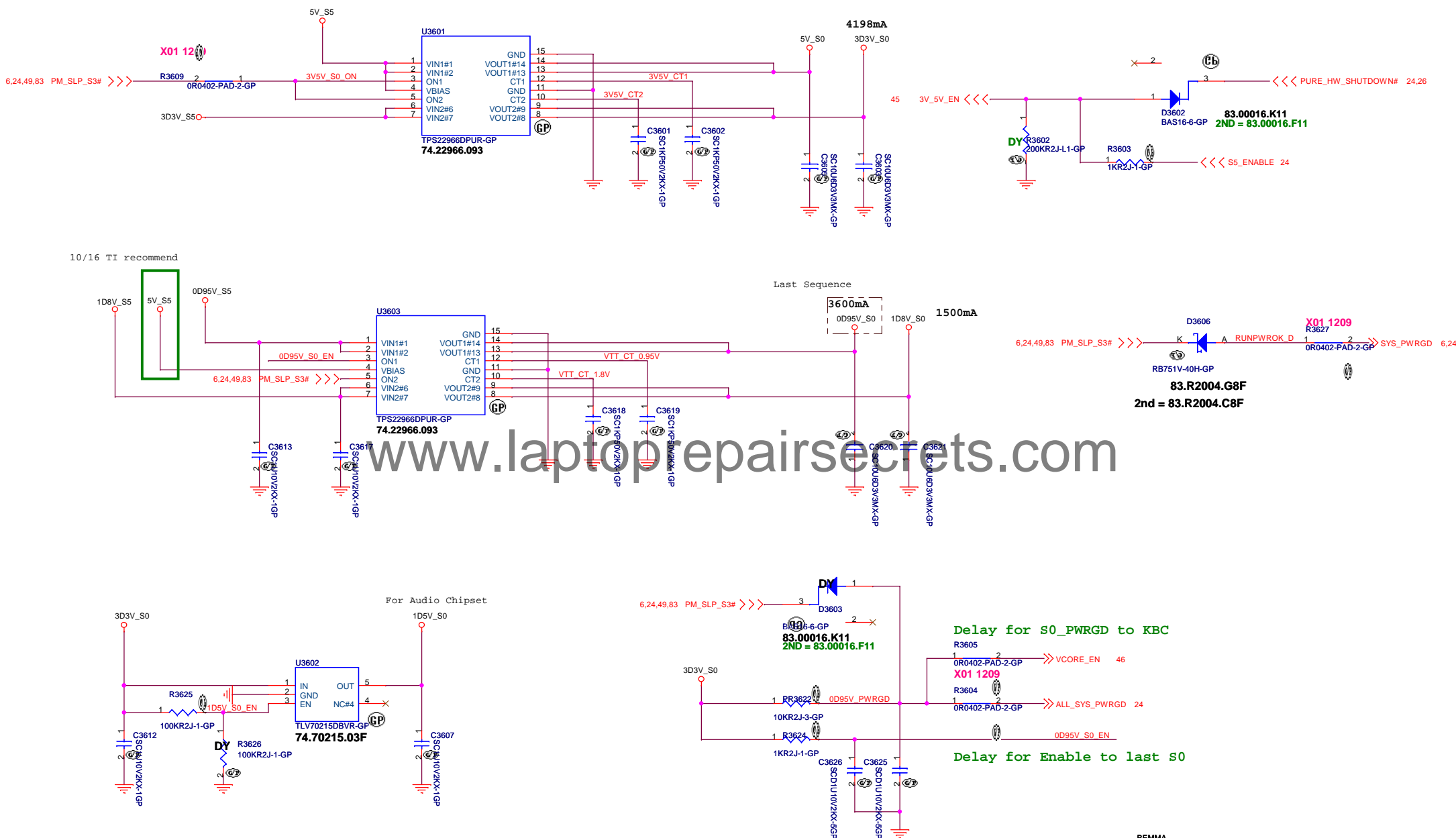
Date: Wednesday, March 05, 2014

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## Power Sequence



SSID = Reset.Suspend

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<b>Reserved</b>					
Size A4	Document Number <b>Janus AMD BEEMA</b>				Rev <b>A00</b>
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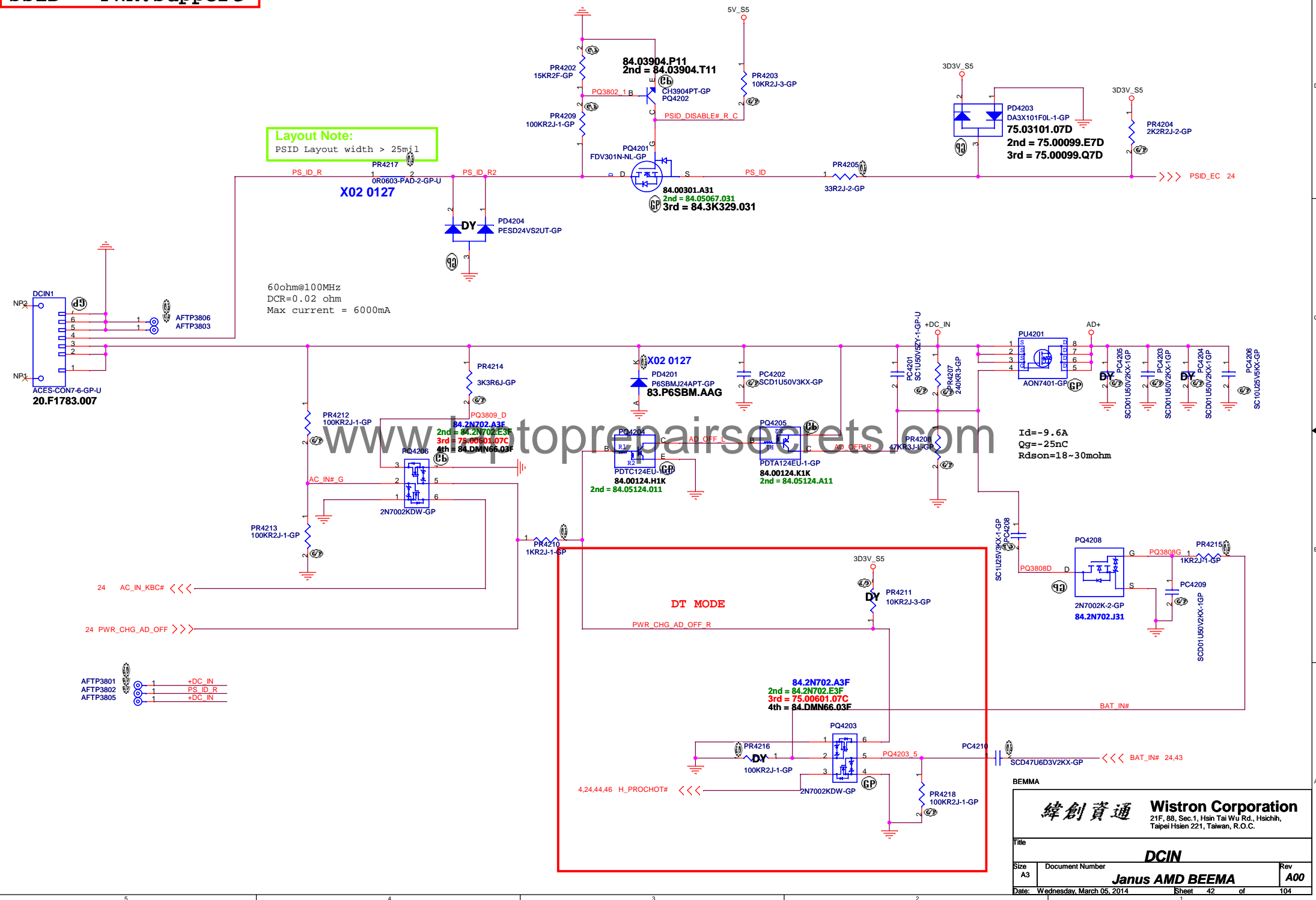
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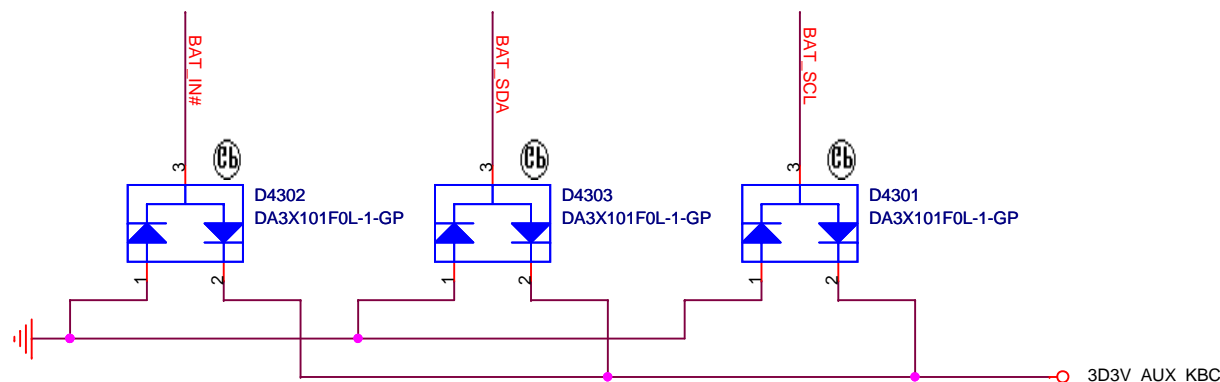
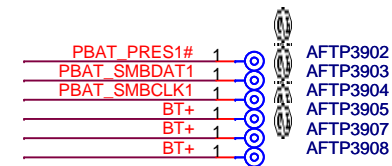
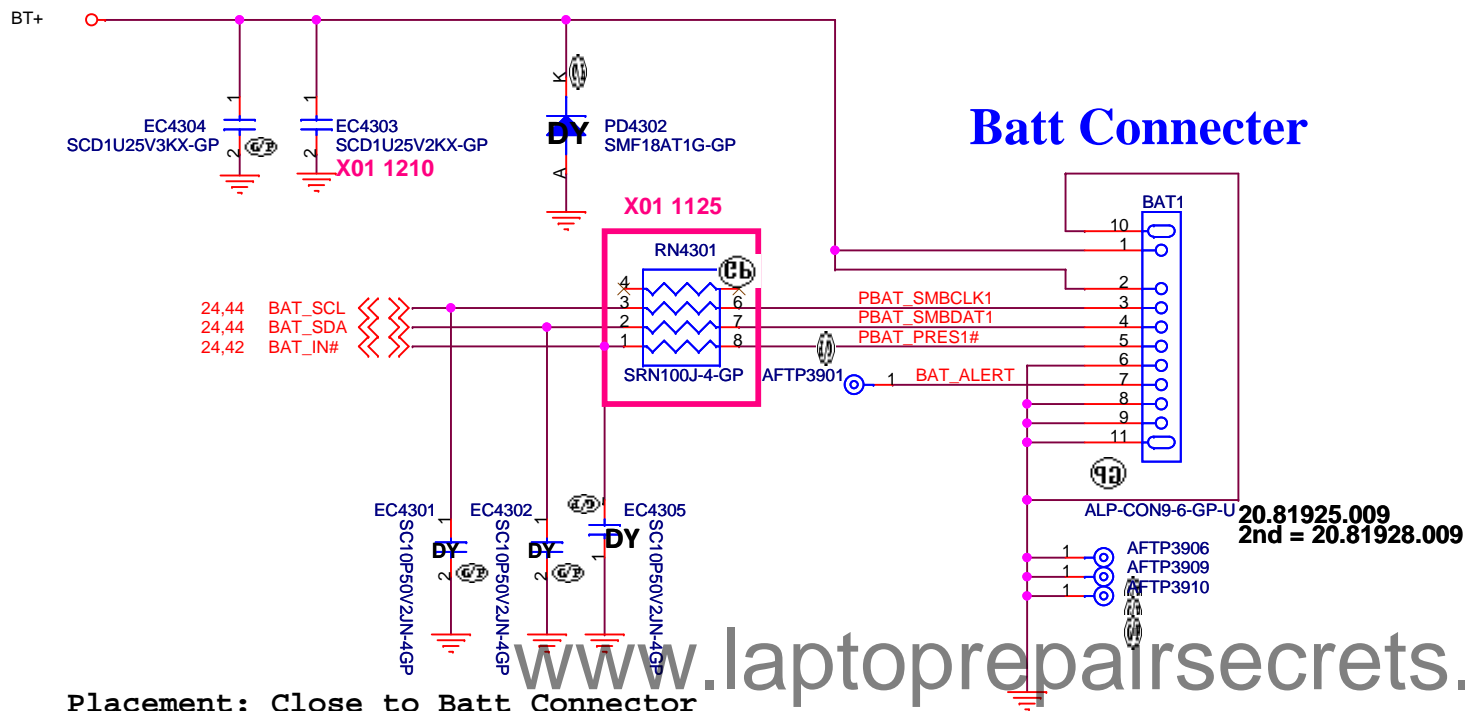
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SSID = PWR.Support



# SSID = PWR.Support



75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

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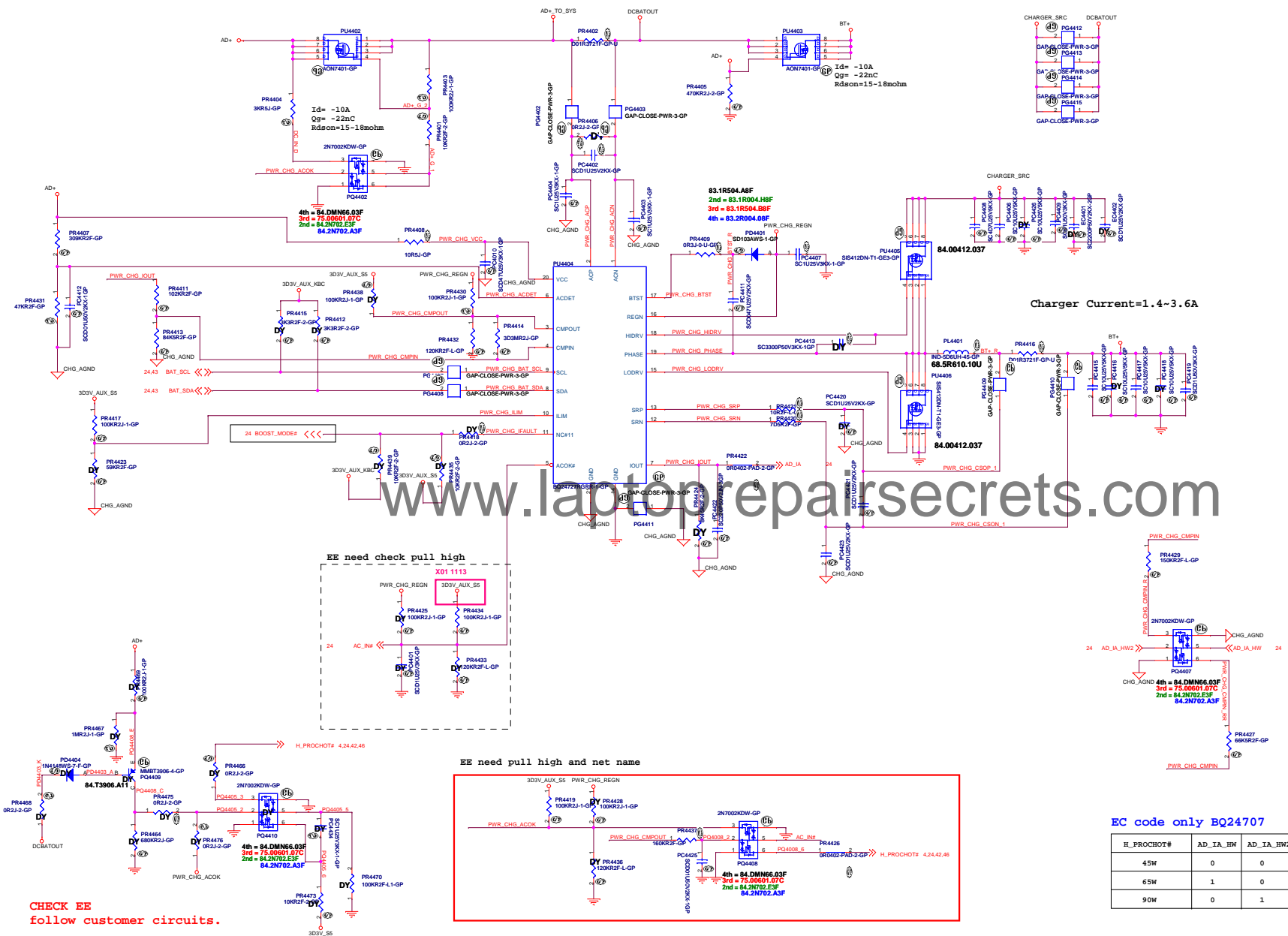
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SSID = Charger



EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

36 3V\_SV\_EN

DCBATOUT

PWR\_DCBATOUT\_5V

5V\_PWR

5V\_S5

Design Current = 8.6A  
12.88A < OCP < 15.46A

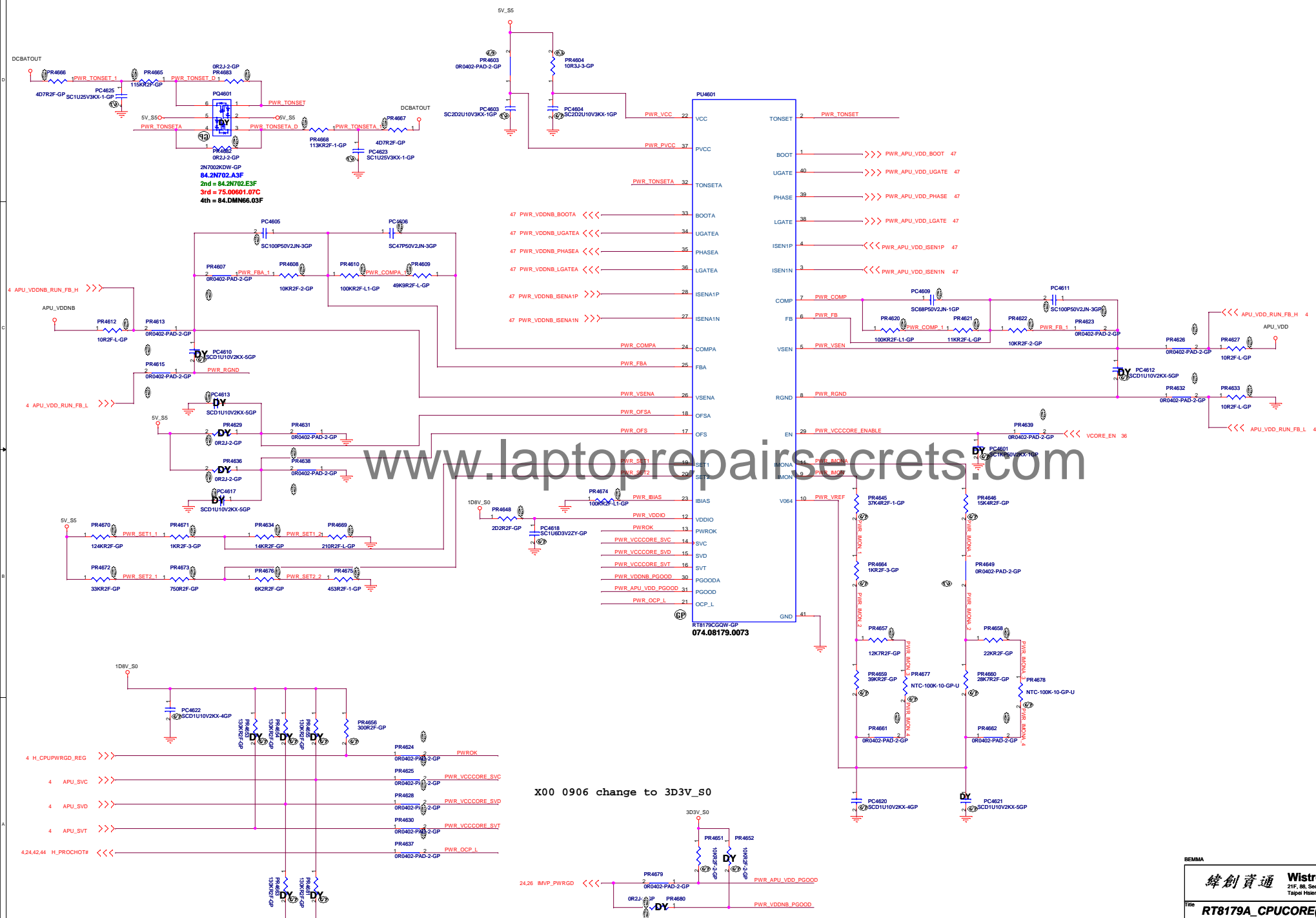
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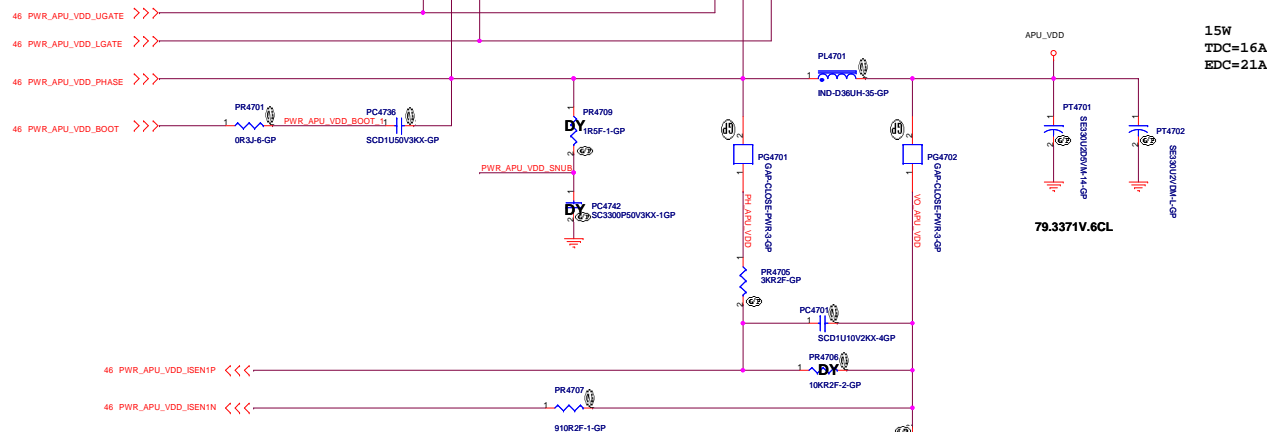
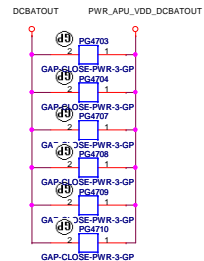
02.51L  
28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
com/ 18mOhm / 79.22710.3KL  
137  
980.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKR 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP EL 220U 6.3V M6.3P4.4 /Chem-i-con/ 18mOhm / 79.22710.3KL  
H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

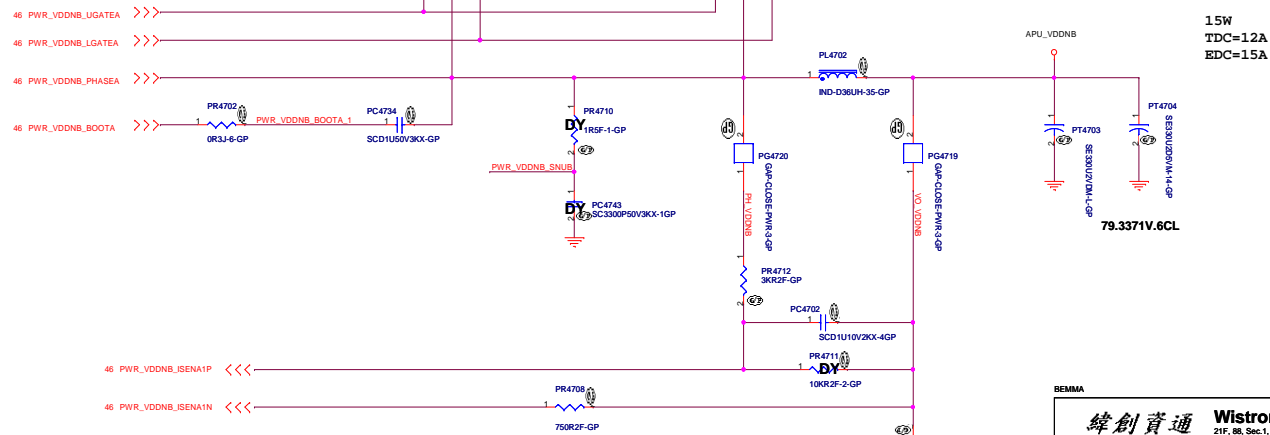
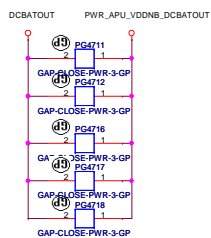
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Inductor: CHIP CHOKE 2.2U 63V PCMC0637-2R2Mn 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP E 220U 6.3V M6.3\*4.4 /Cheml-con/ 18mohm/ 79.22710.3KL  
H/S:SiS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037  
L/S:SiS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

```
SSID = CPU.Regulator
```



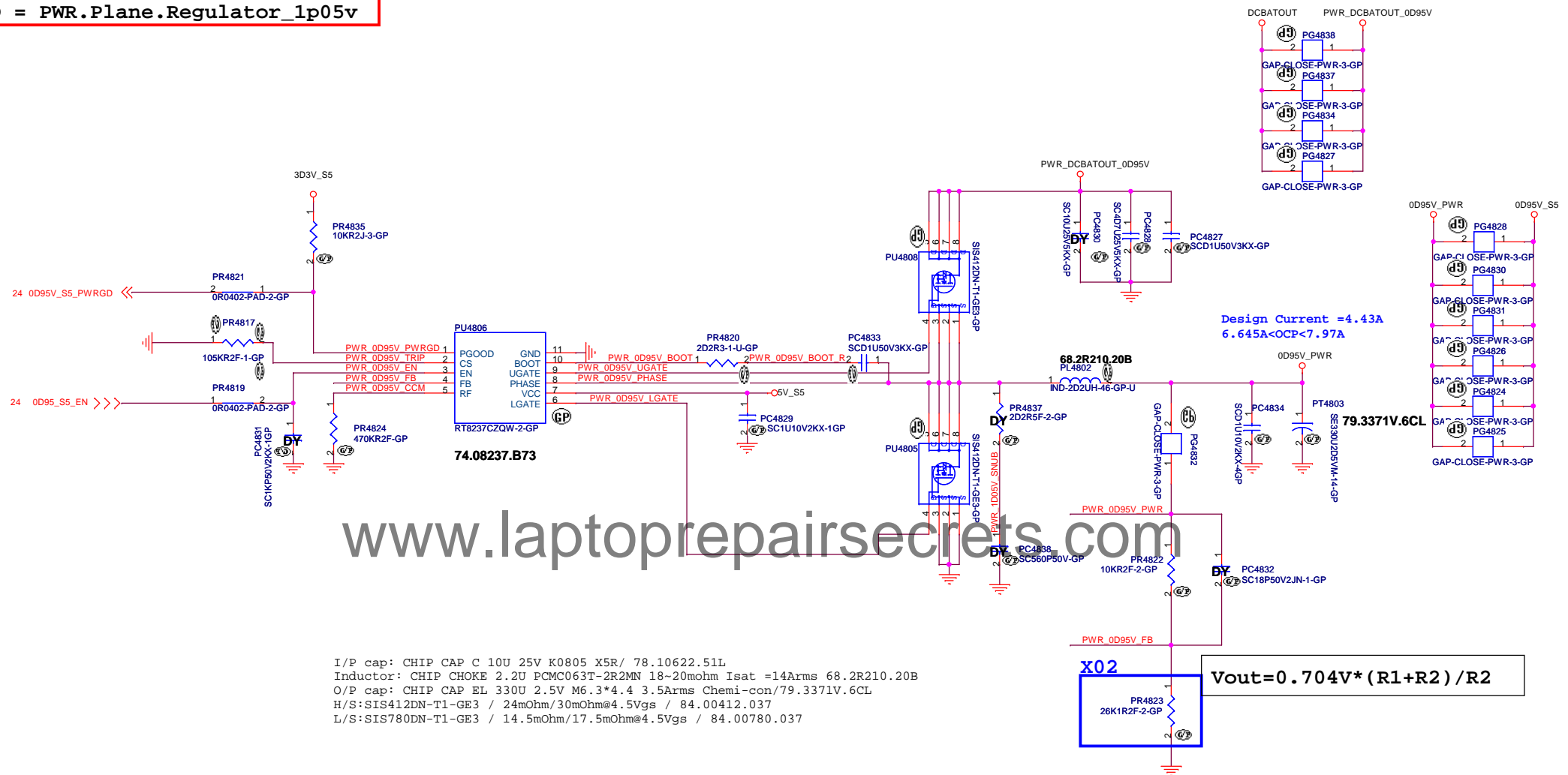


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I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKE 0.36UH PCME064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W  
O/P cap:CHIP CAP 470UF 2V EEF5X0D471X /Panasonic/ 6mOhm / 79.47719.2BL  
Dual N FET MOS SI2920DT-T1-GE3 DUAL NC POWER 8P /H/S 7.4mohm/8.9mohm / L/S 2.9mOhm/3.5mohm@4.5Vgs / 84.00920.037

```
SSID = PWR.Plane.Regulator_1p05v
```

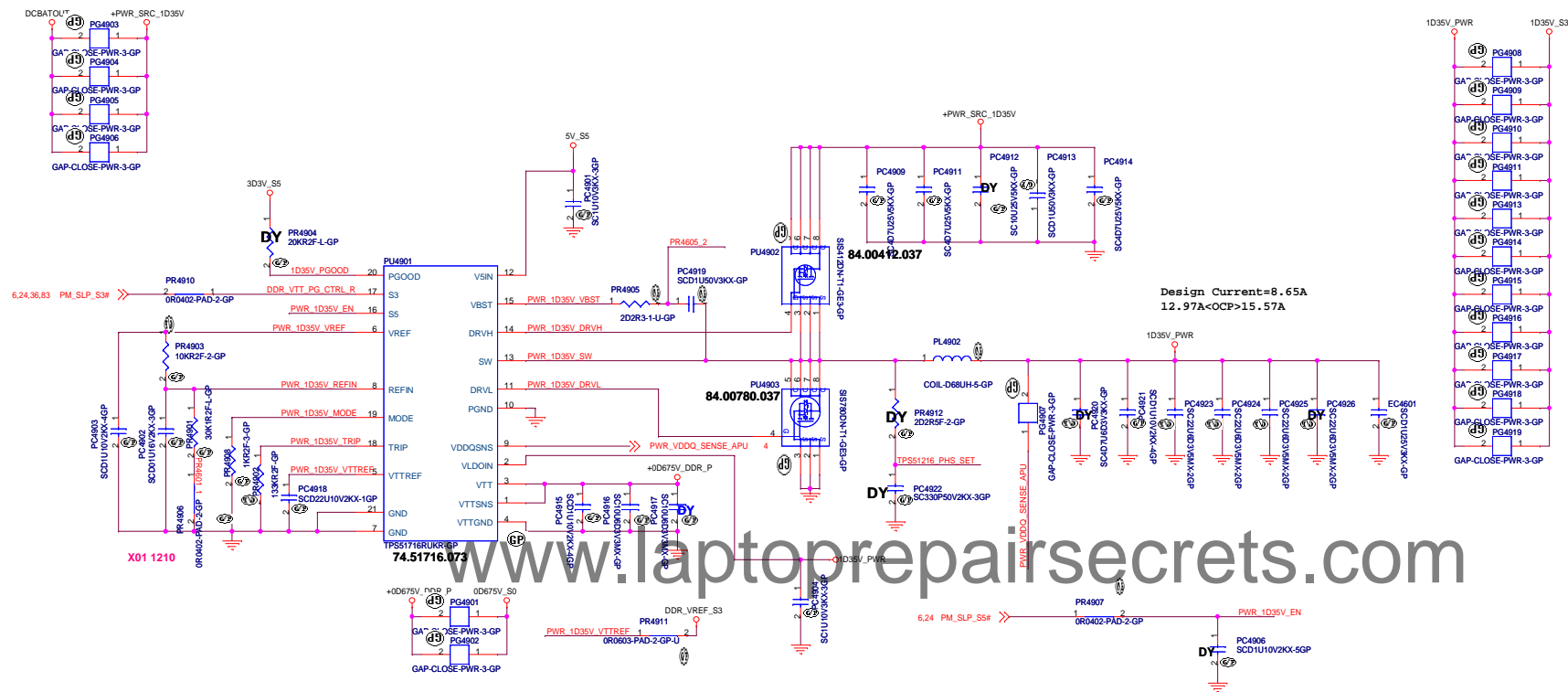


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKe 2.2U PCMC063T-2R2MN 18-20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP EL 330U 2.5V M6.3\*4.4 3.5Arms Chemi-con/79.3371V.6CL  
H/S: SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S: SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$



```
SSID = PWR.Plane.Regulator 1p35v0p675v
```



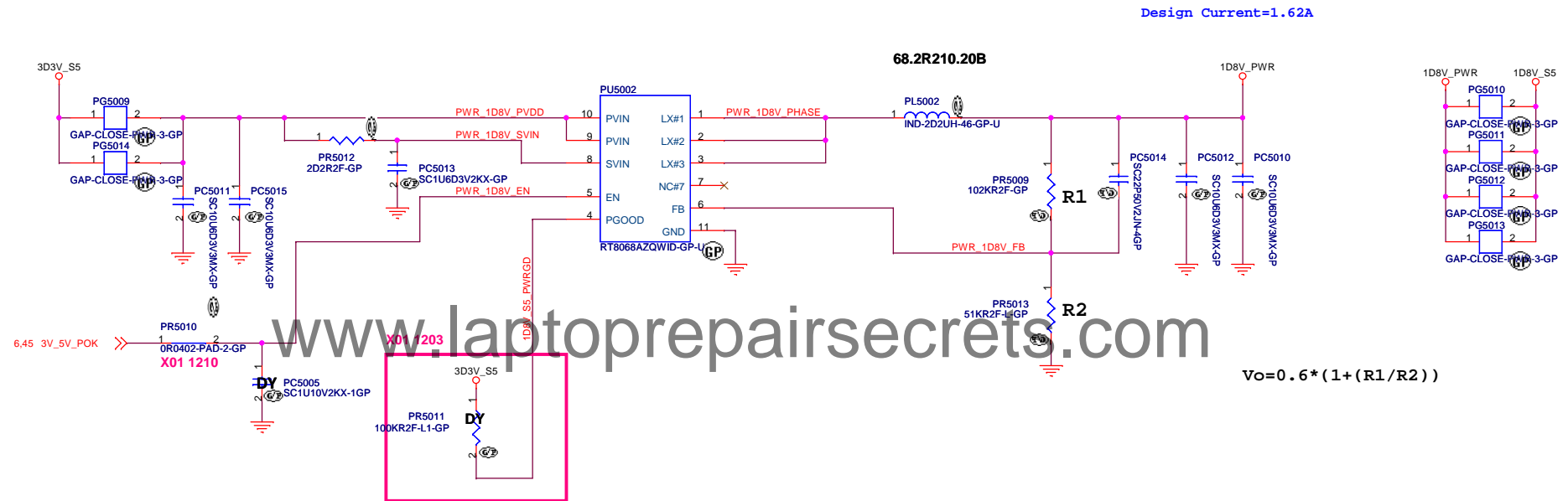
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

```
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037
```

TPS571716 MODE		
PR4608	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

SSID = PWR.Plane.Regulator\_1p8v

## RT8068A for 1D8V\_S5



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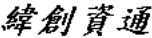
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Title			RT8068A 1D8V_S5
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SSID = PWR.Plane.Regulator\_1p5v

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Title <b>TLV70215_1D5</b>			
Size A3	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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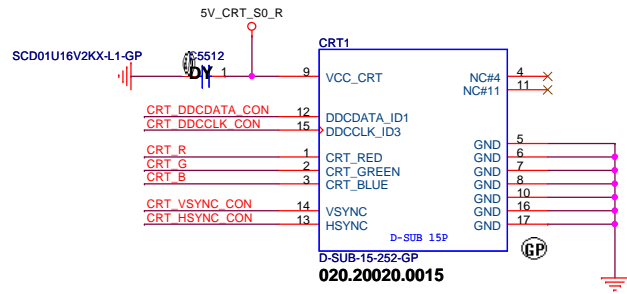
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SSID = VIDEO

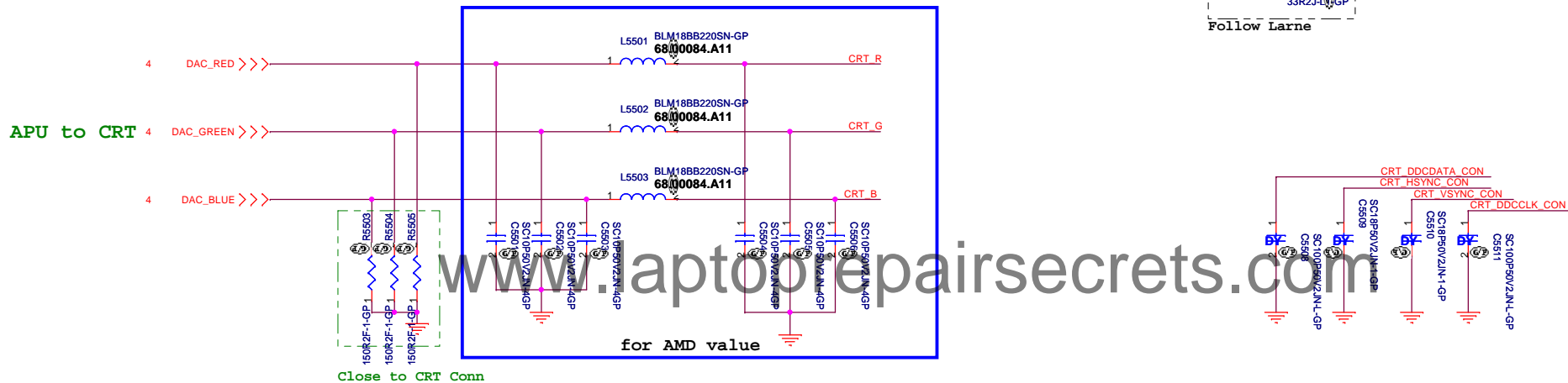
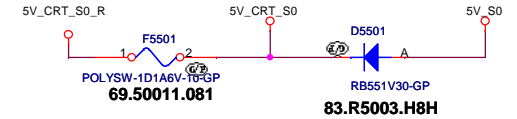
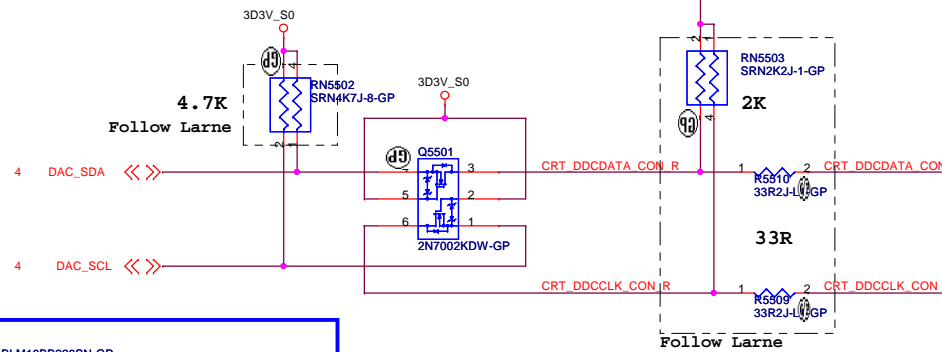
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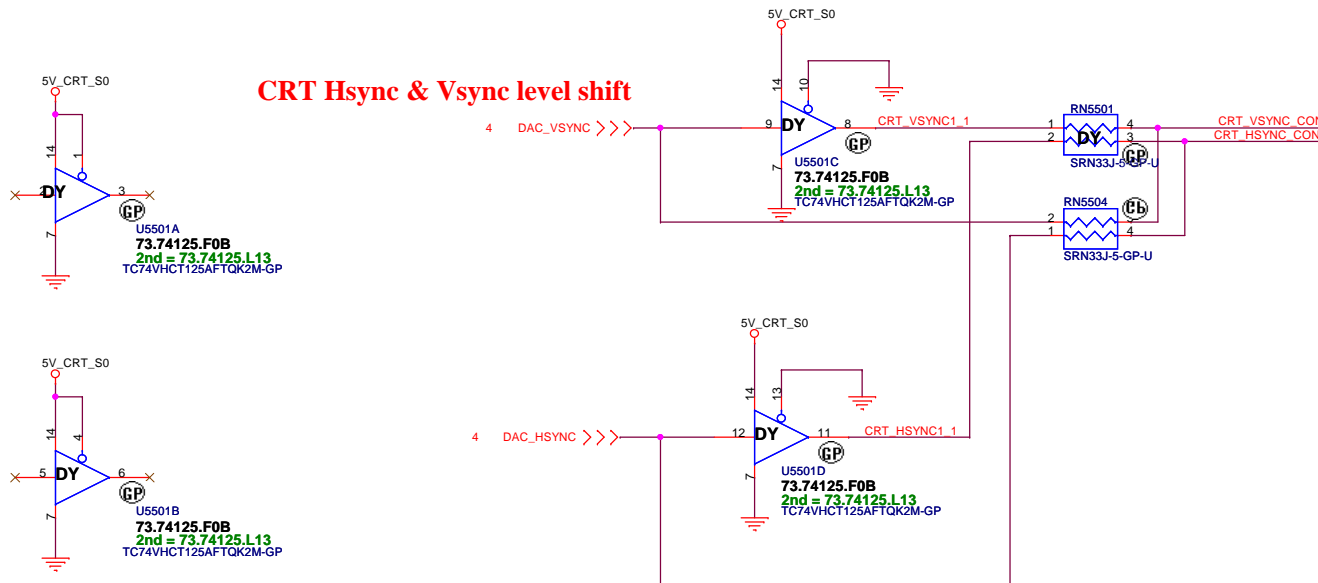
# CRT Board Connector



## CRT DDCDATA & DDCCLK level shift

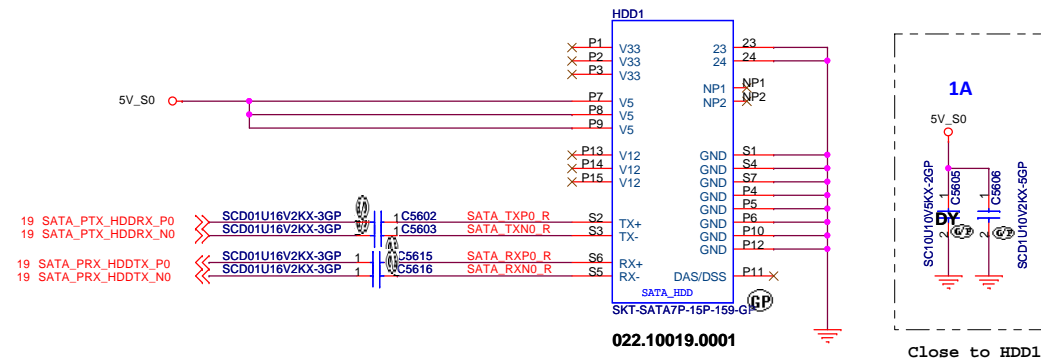


## CRT Hsync & Vsync level shift

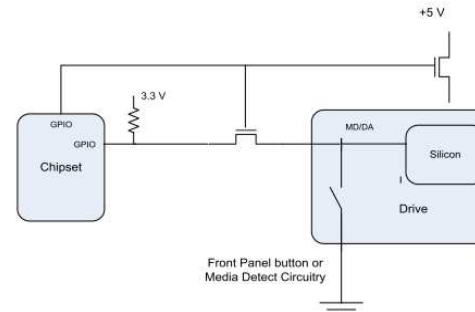
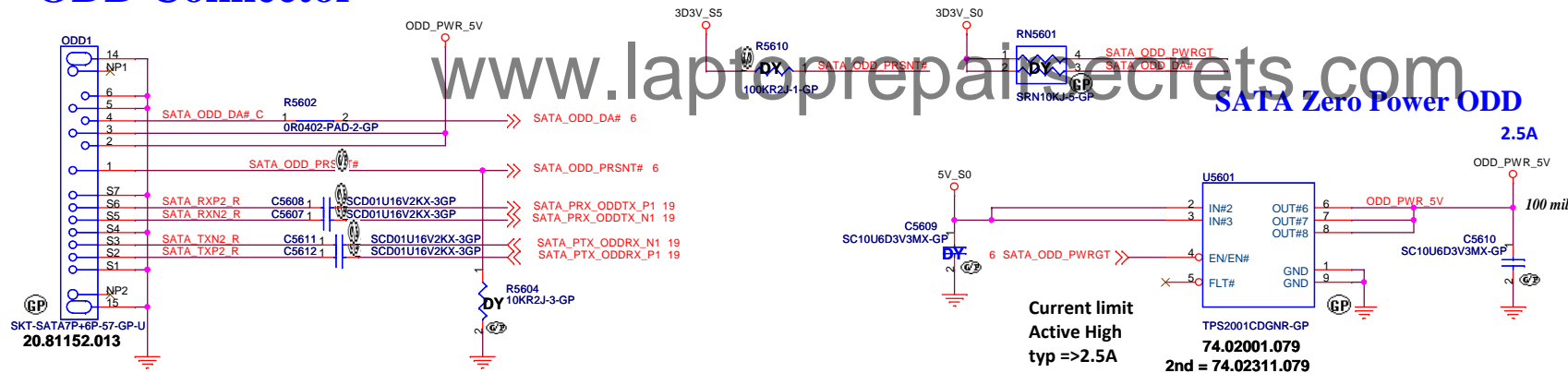


SSID = SATA

## SATA HDD Connector



## ODD Connector



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HDD/ODD			
Size A3	Document Number	Rev	A00
Janus AMD BEEMA			
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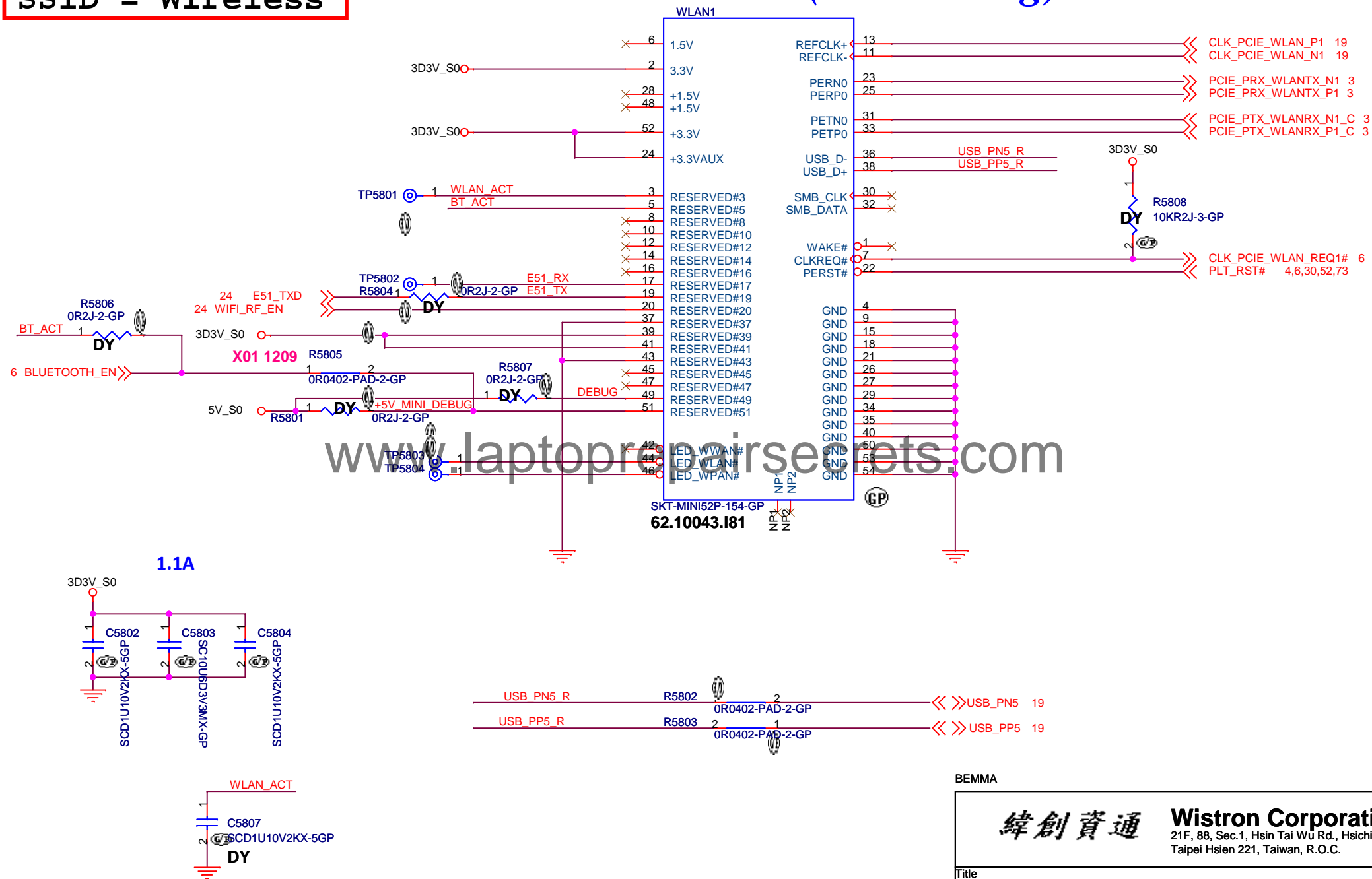


SSID = ESATA

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# SSID = Wireless

## *Mini Card Connector(802.11a/b/g)*



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Title
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**WLAN CONN**

Size	A4
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Document Number

## Janus AMD BEEMA

Rev	<b>A00</b>
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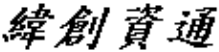
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
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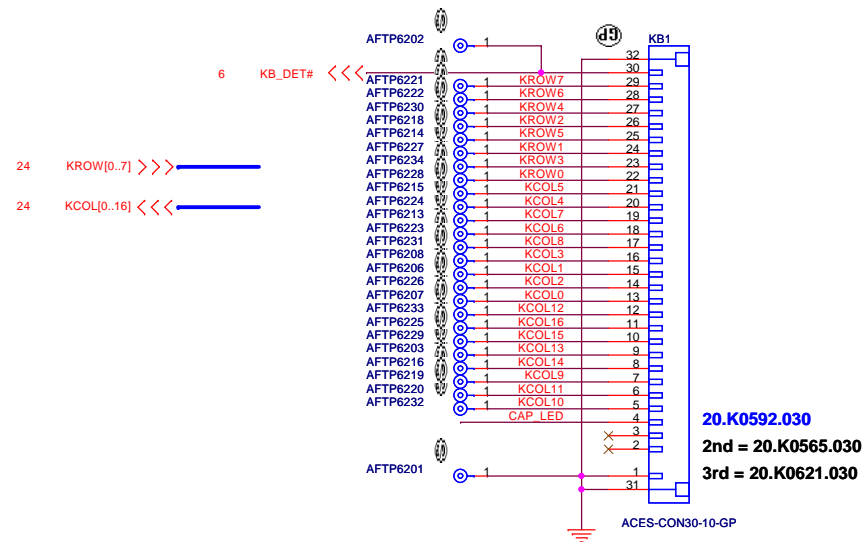
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Title <b>(Reserved)</b>		
Size A4	Document Number <b>Janus AMD BEEMA</b>	Rev <b>A00</b>
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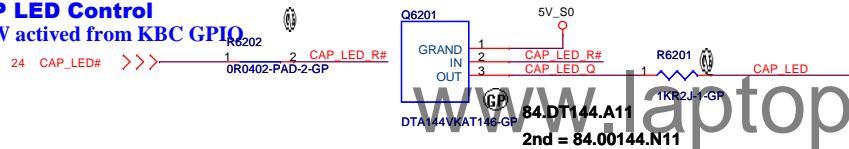


**SSID = KBC**

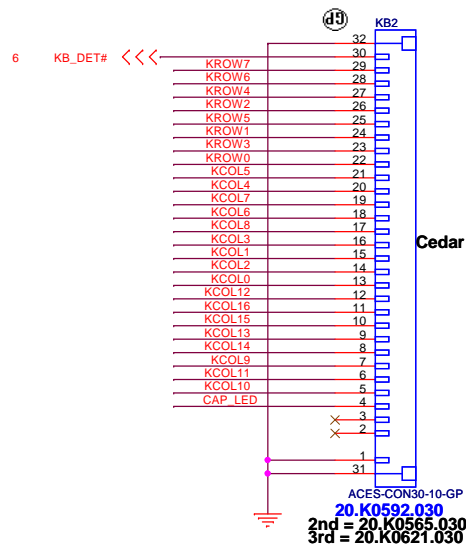
## Internal Keyboard Connector (DVC40)



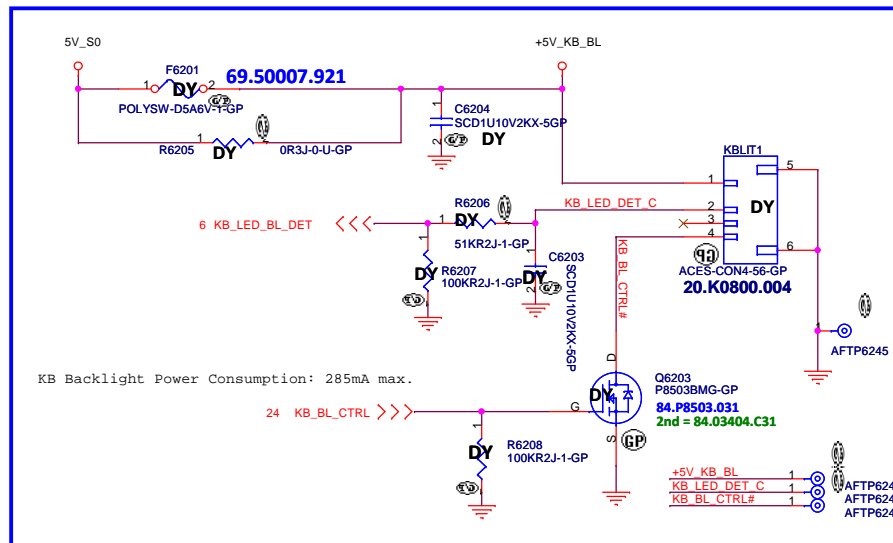
**CAP LED Control**  
LOW actived from KBC GPIO



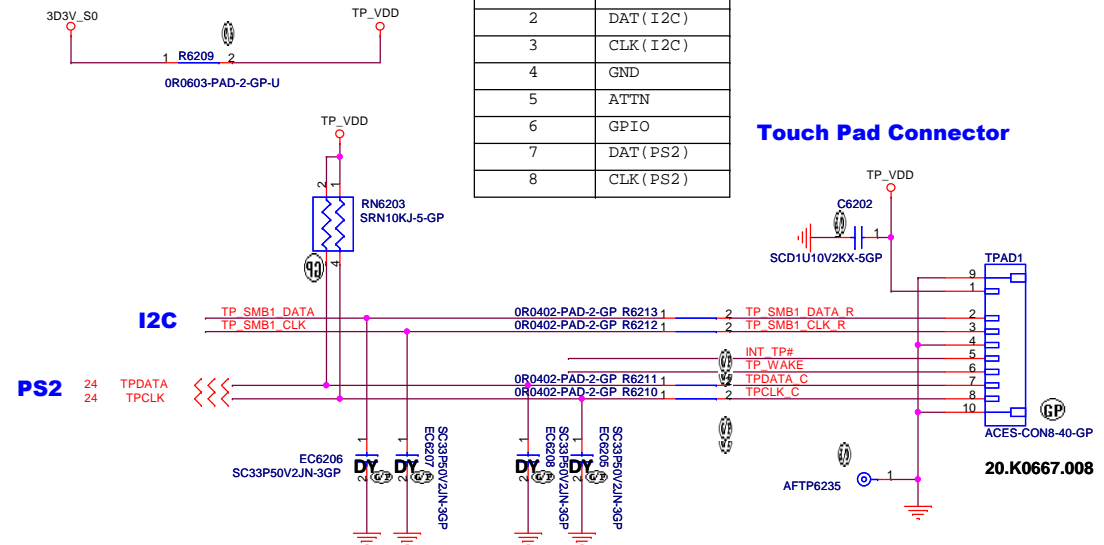
## Internal Keyboard Connector (DVC50)



## Keyboard Backlight (DVC50)

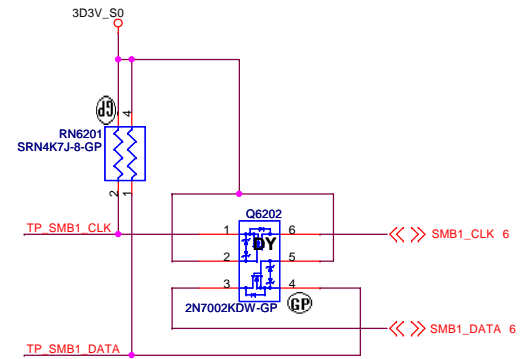


```
SSID = Touch.Pad
```



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

## Touch Pad Connector



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### Key Board/Touch Pad

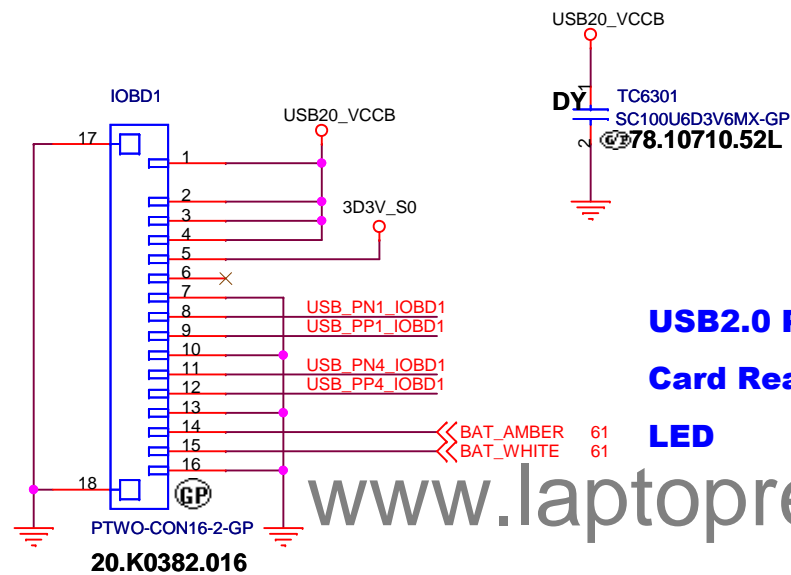
Size  
A3

Document Number

**Janus AMD BEEMA**

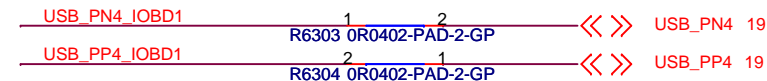
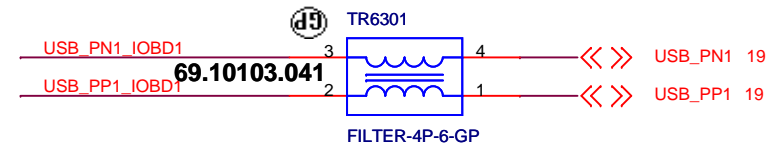
Date: Wednesday, March 05, 2014

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## USB2.0 Port3 Card Reader LED

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The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

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Title

**IO Board Connector**

Size  
A4

Document Number

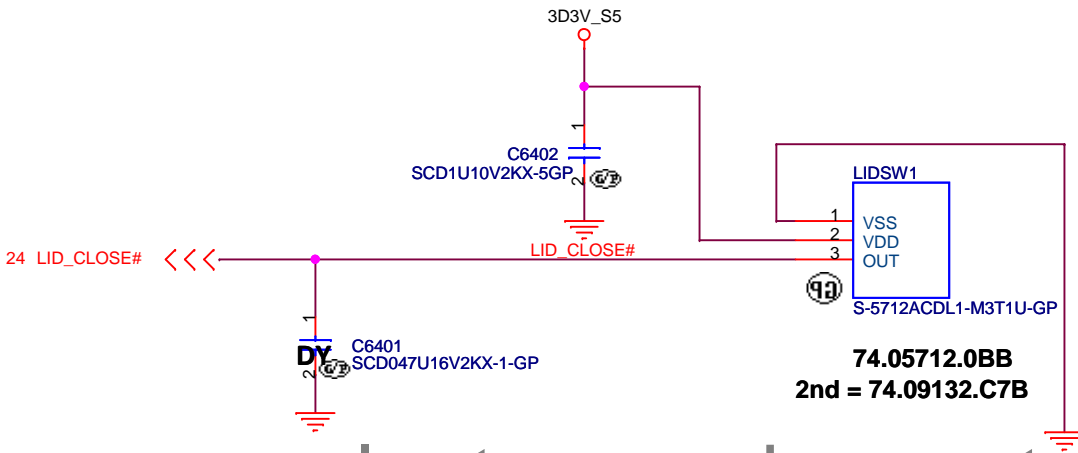
**Janus AMD BEEMA**

Rev  
A00

Date: Wednesday, March 05, 2014

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SSID = User.Interface



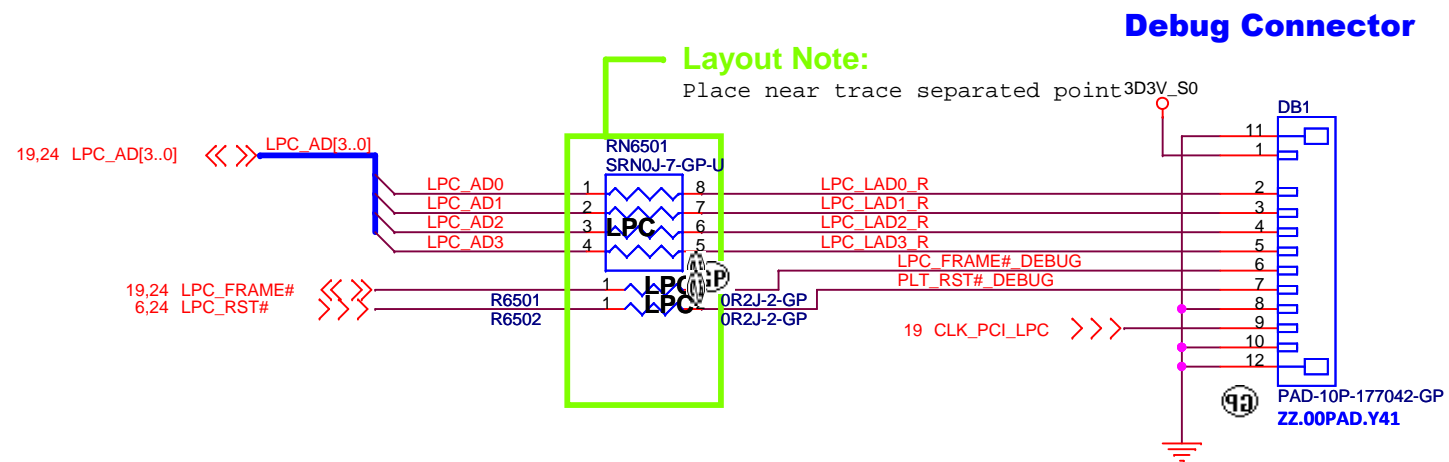
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Title			
<b>Hall Sensor</b>			
Size A4	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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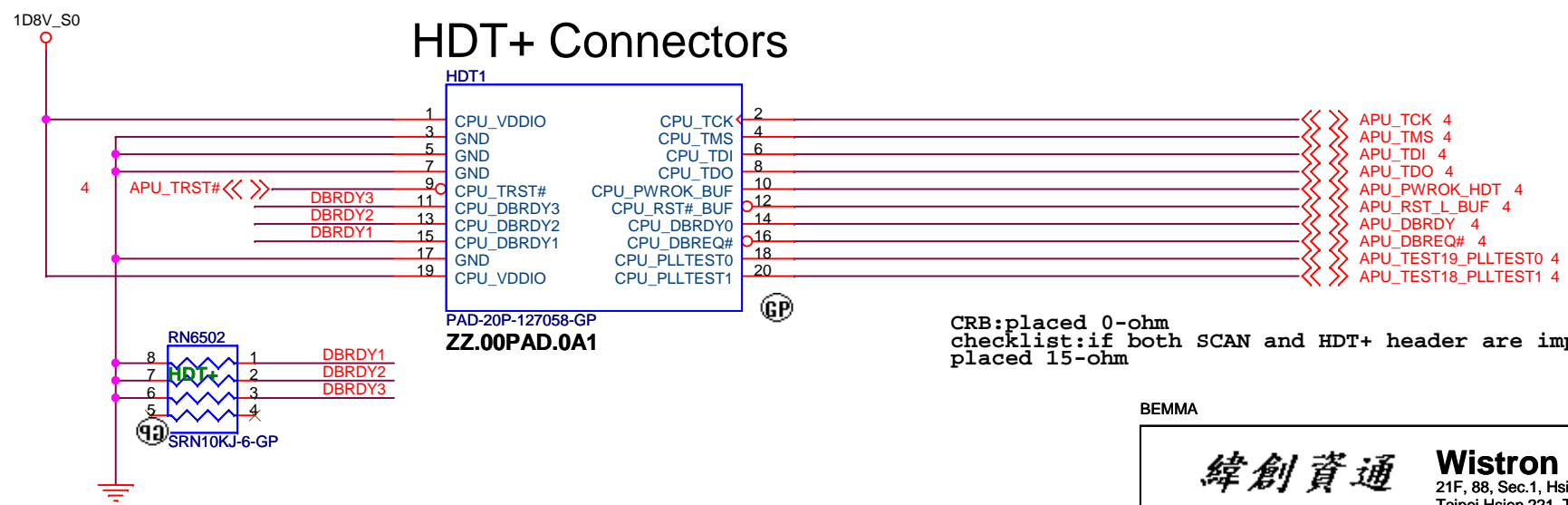
SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41  
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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HDT+ Connectors



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Title <b>Dubug connector</b>		
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Title

**Reserved**

Size  
A3

Document Number  
**Janus AMD BEEMA**

Rev  
**A00**

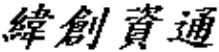
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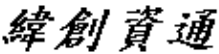
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Title <b>Thunderbolt (1/5)</b>			
Size A4	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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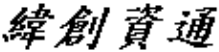
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Title <b>Thunderbolt (2/5)</b>			
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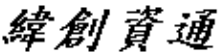
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Title			
<b>Thunderbolt (3/5)</b>			
Size	Document Number		Rev
A4	<b>Janus AMD BEEMA</b>		<b>A00</b>
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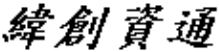
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Title <b>Thunderbolt (4/5)</b>			
Size A4	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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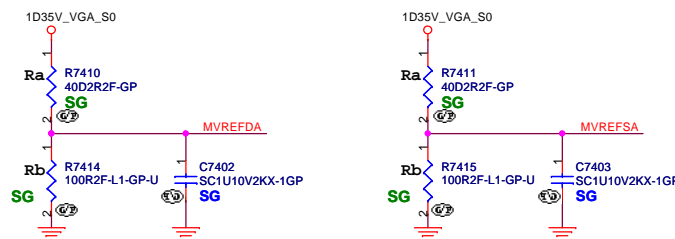
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Size A4	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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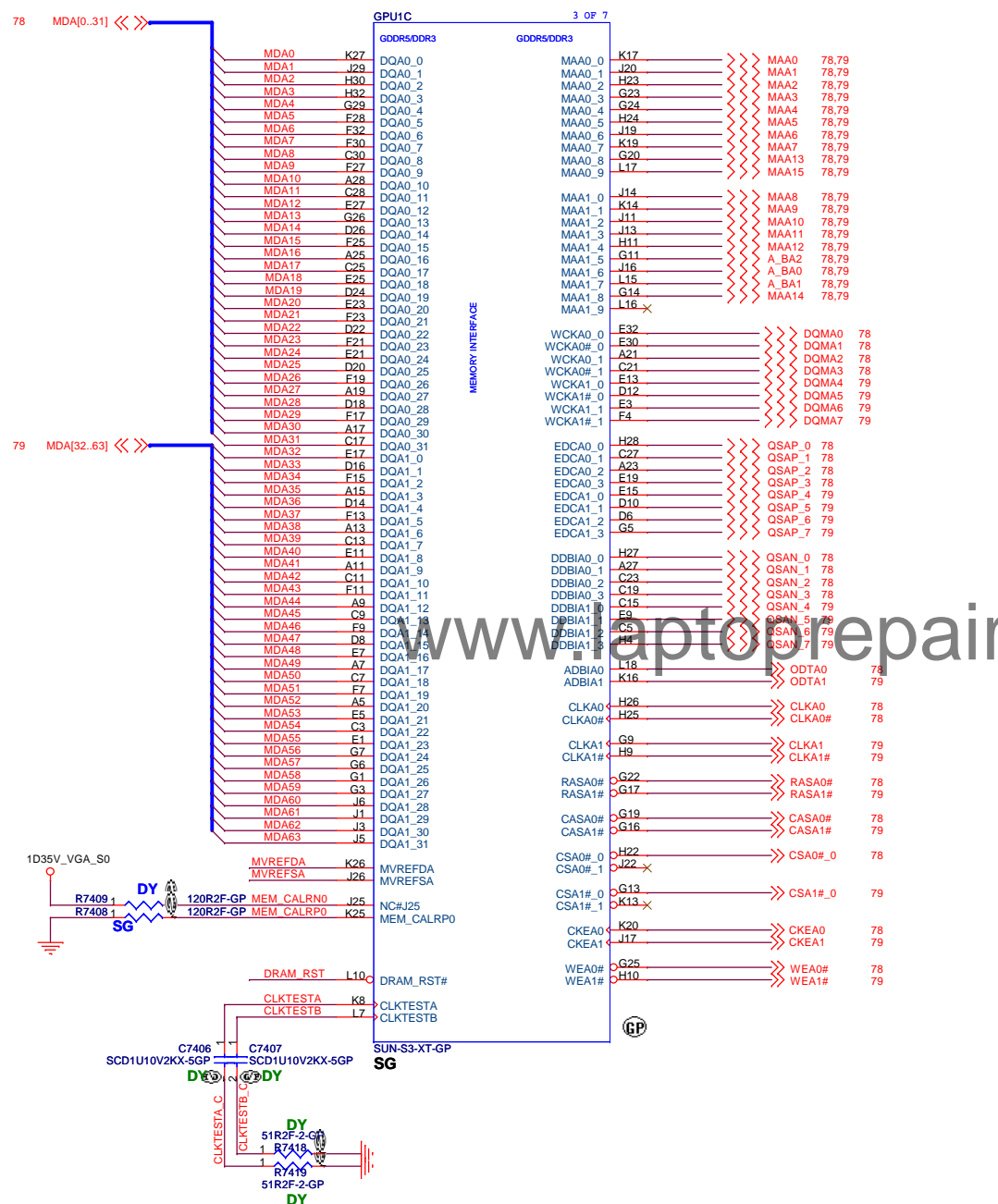
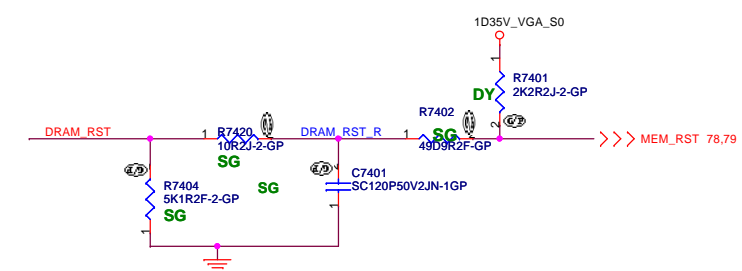


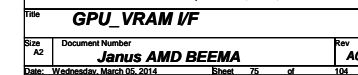
# PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



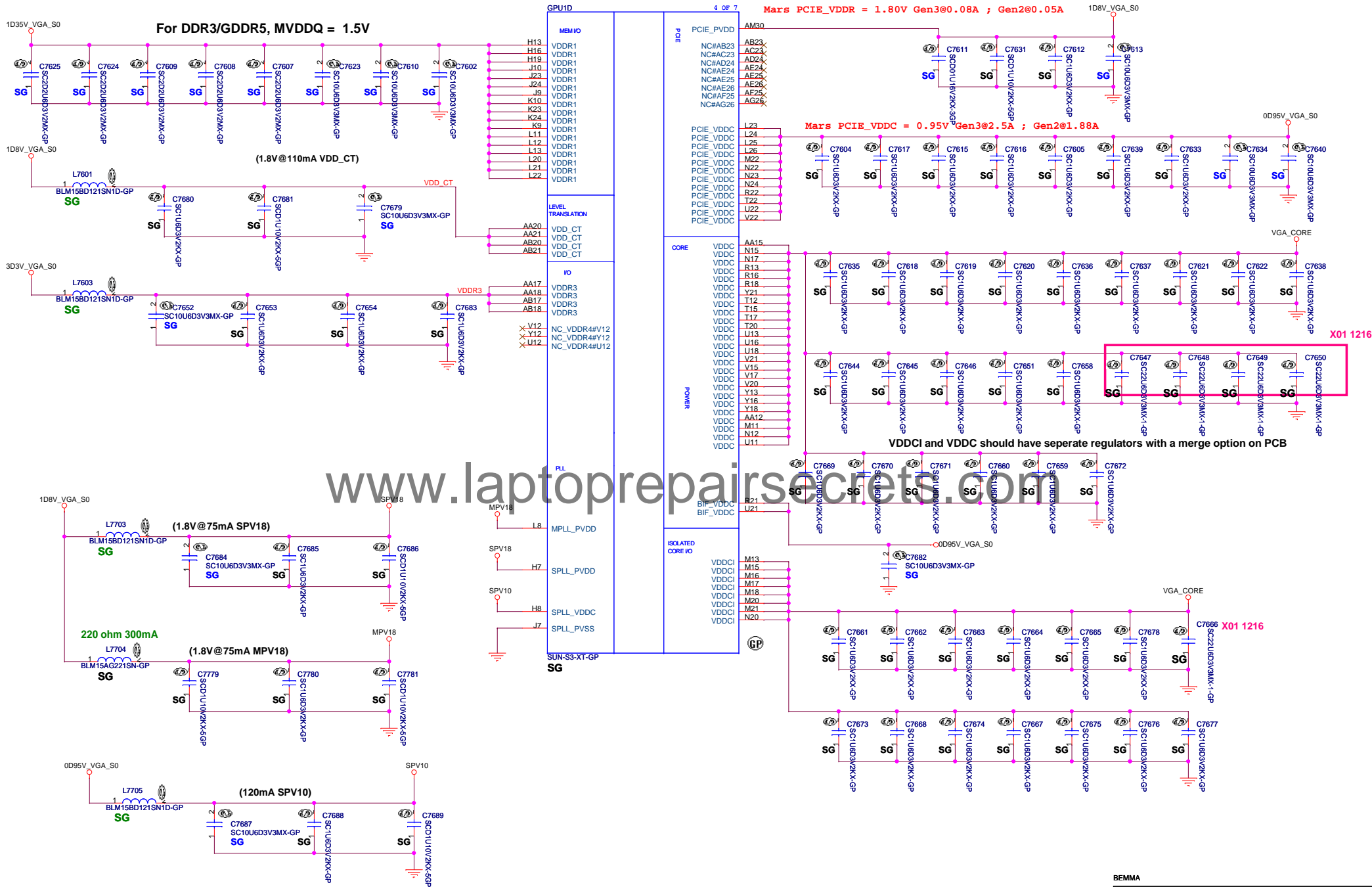
## DDR3/GDDR3 Memory Stuff Option(Mad/Park)

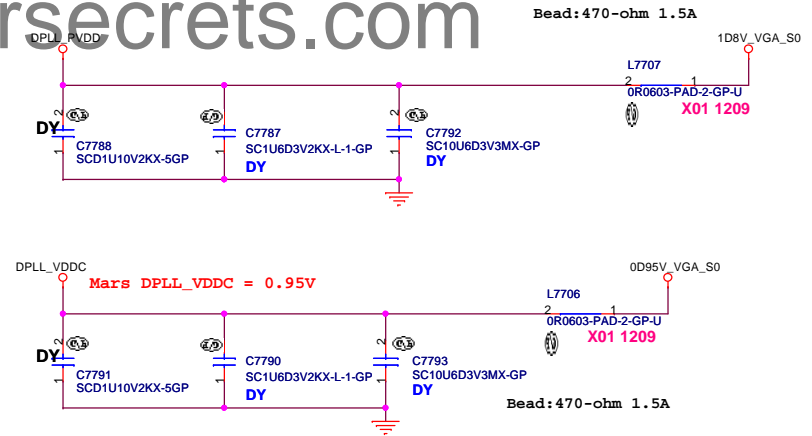
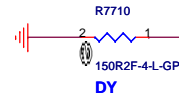
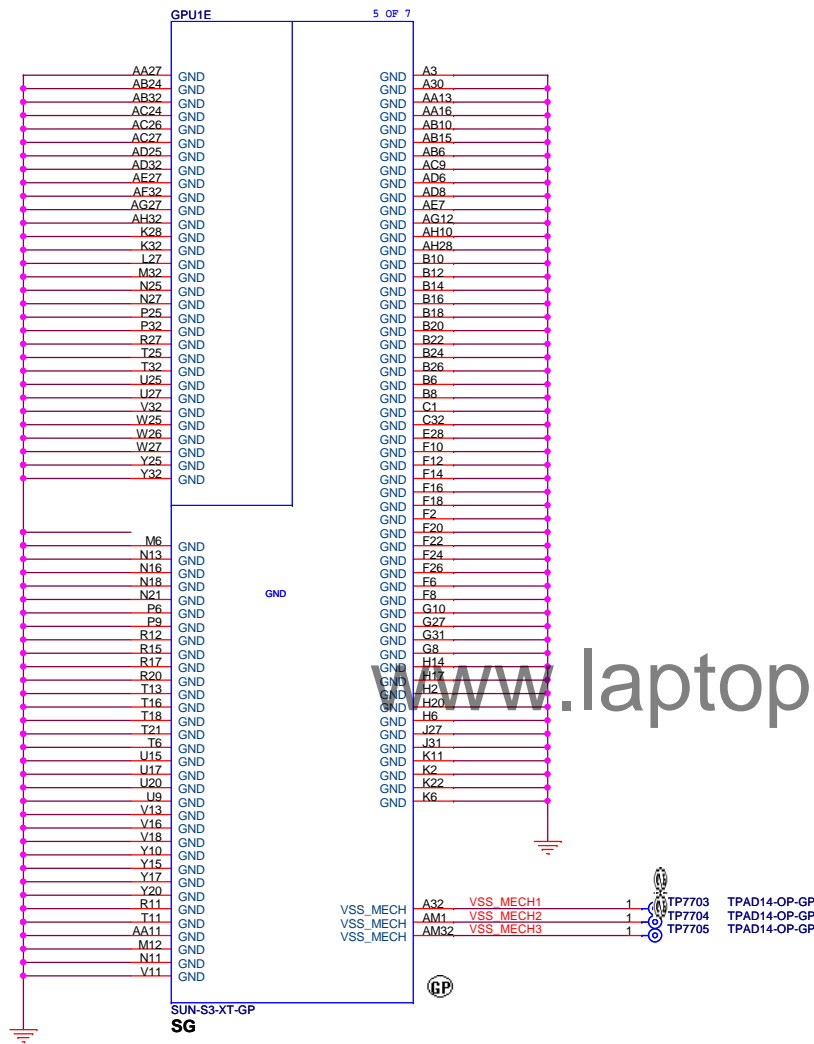
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.35V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R





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Title GPU\_POWER/GND

Size Project Name

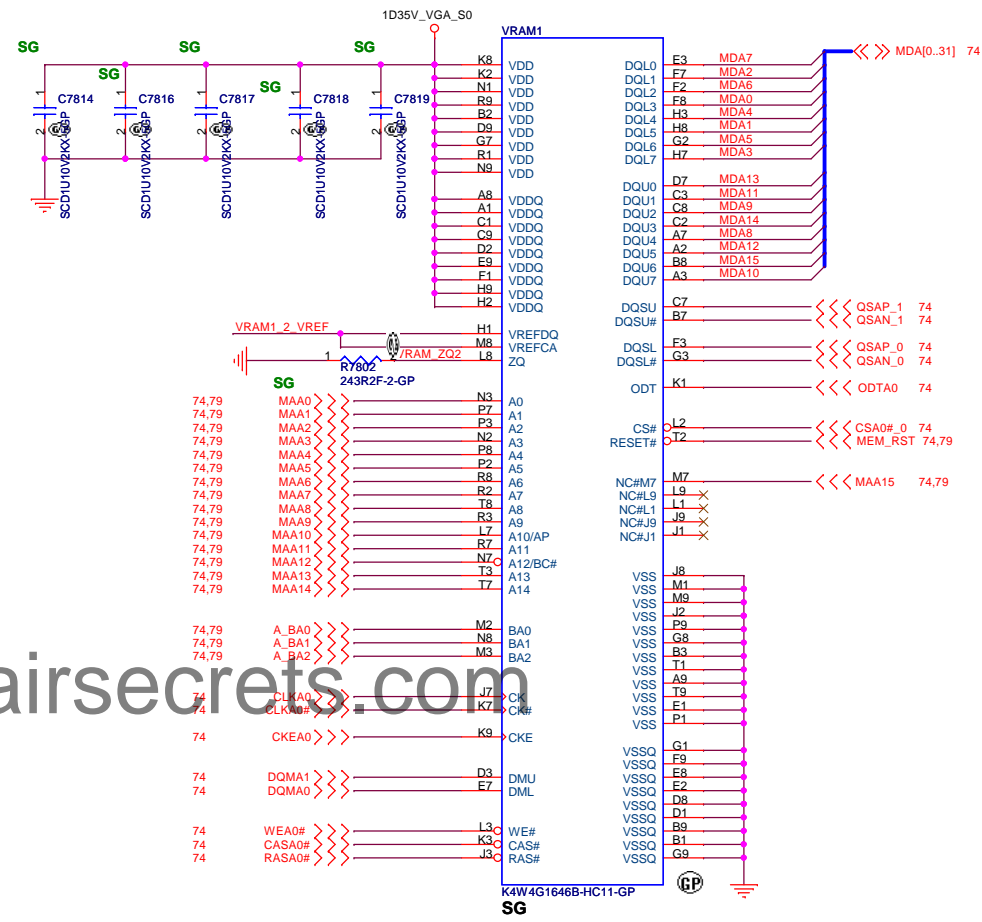
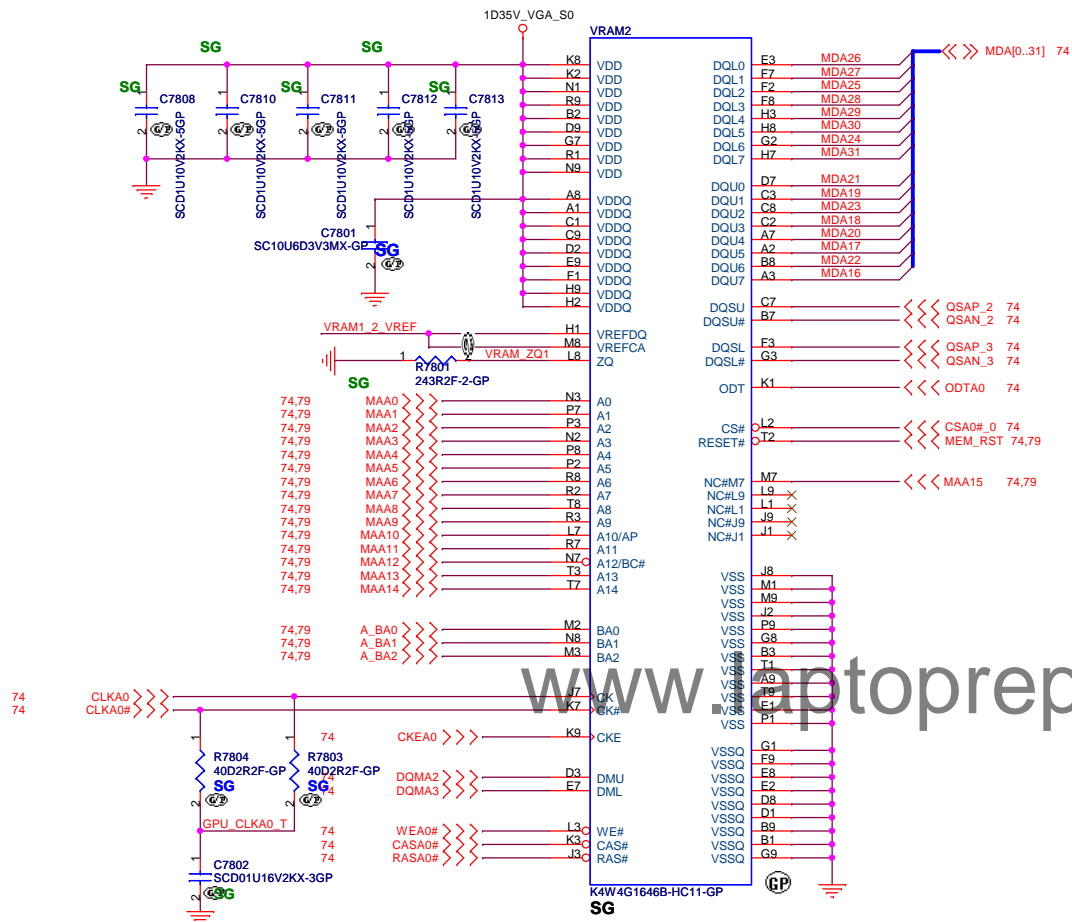
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Rev

<Project Name>

<Rev>



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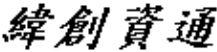
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Title		
GPU-VRAM1,2 (1/4)		
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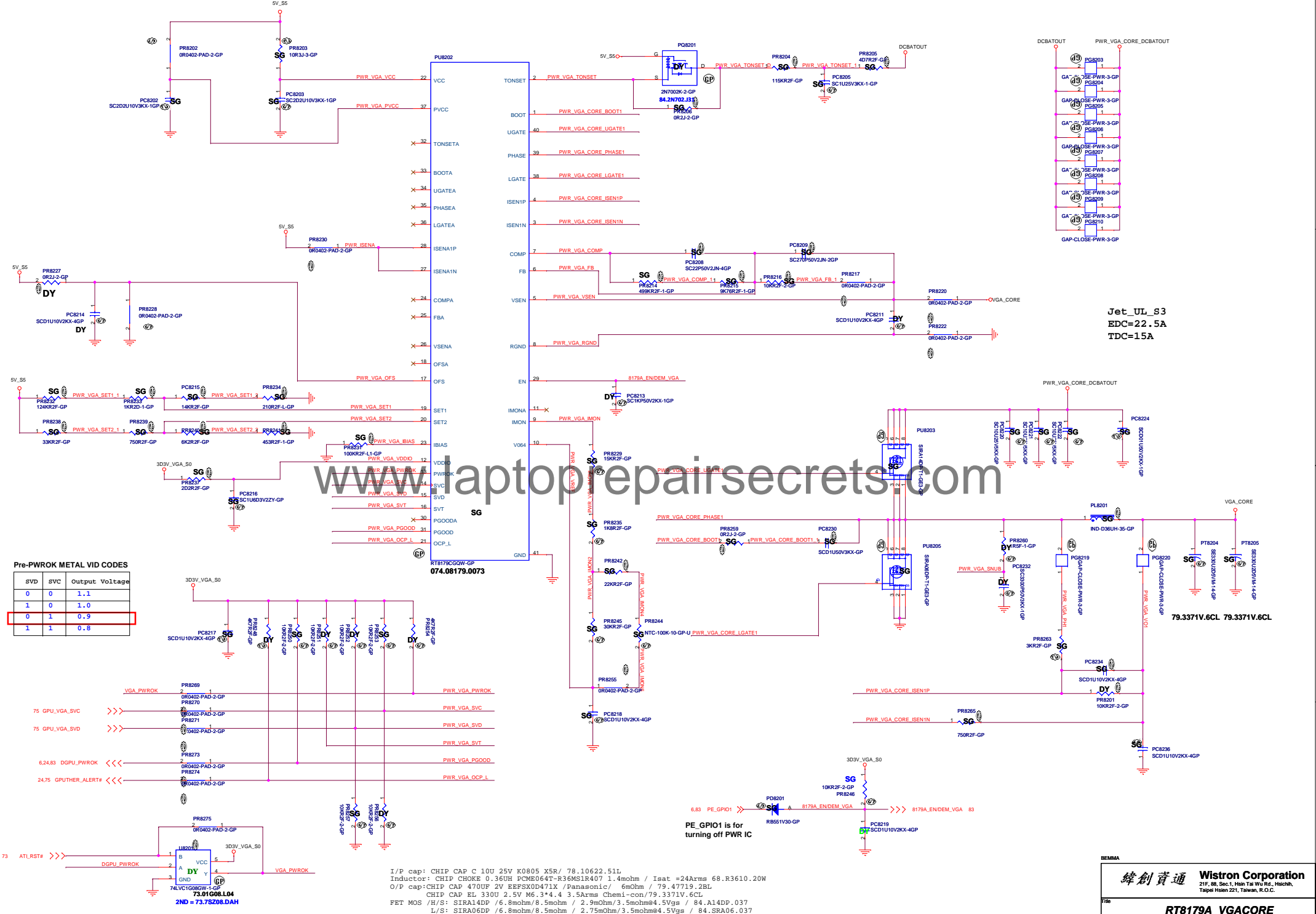
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Size A4	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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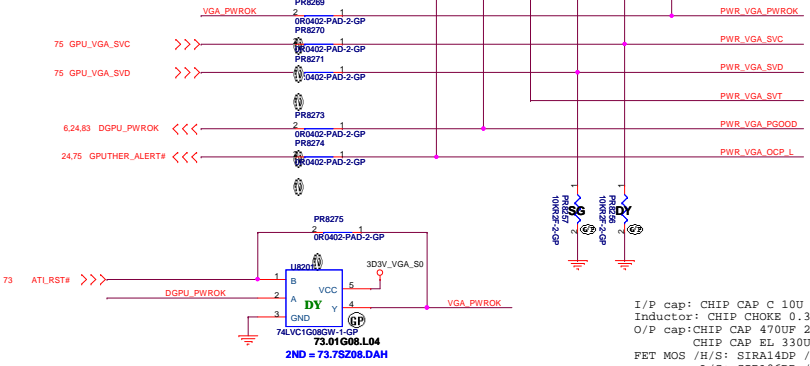
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Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKO 0.36UH DCMB064T-R36M51R407 1.4mohm / Isat =24Arms 68.R3610.20W  
O/P cap: CHIP CAP 470UF 2V EEPX00471X / Panasonic / 79.47719.2BL  
CHIP CAP EL 330U 2.5V M6.3\*4.4 3.5Arms Chemi-con/79.3371V.6CL  
FET MOS /H/S: SIRA14DP /6.8mohm/8.5mohm / 2.9mohm/3.5mohm@4.5Vgs / 84.A14DP.037  
L/S: SIRA06DP /6.8mohm/8.5mohm / 2.75mohm/3.5mohm@4.5Vgs / 84.SRA06.037

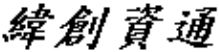
Jet\_UL\_S3  
EDC=22.5A  
TDC=15A

79.3371V.6CL 79.3371V.6CL



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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Janus AMD BEEMA</b>		Rev <b>A00</b>
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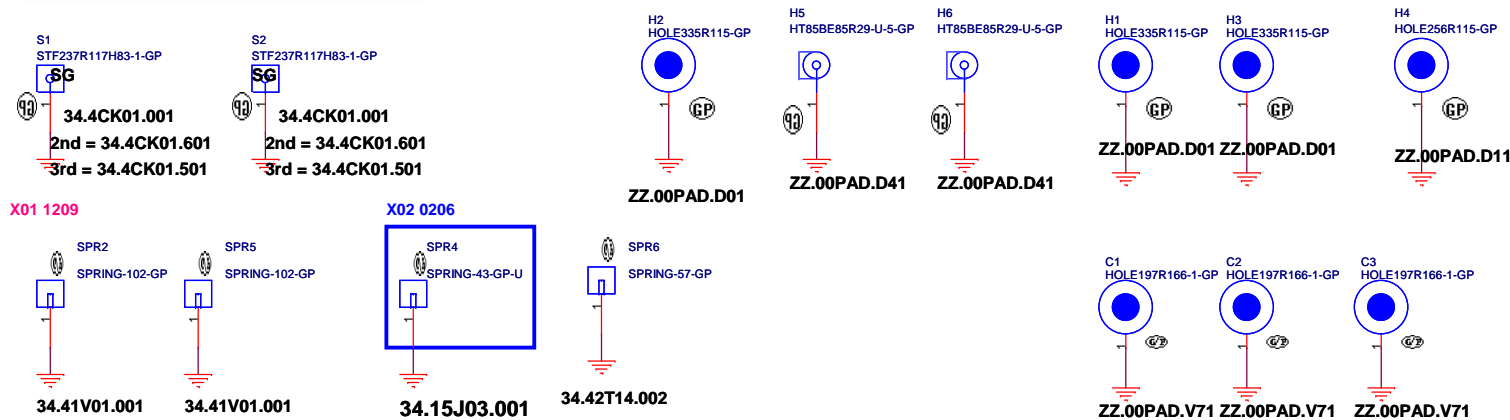
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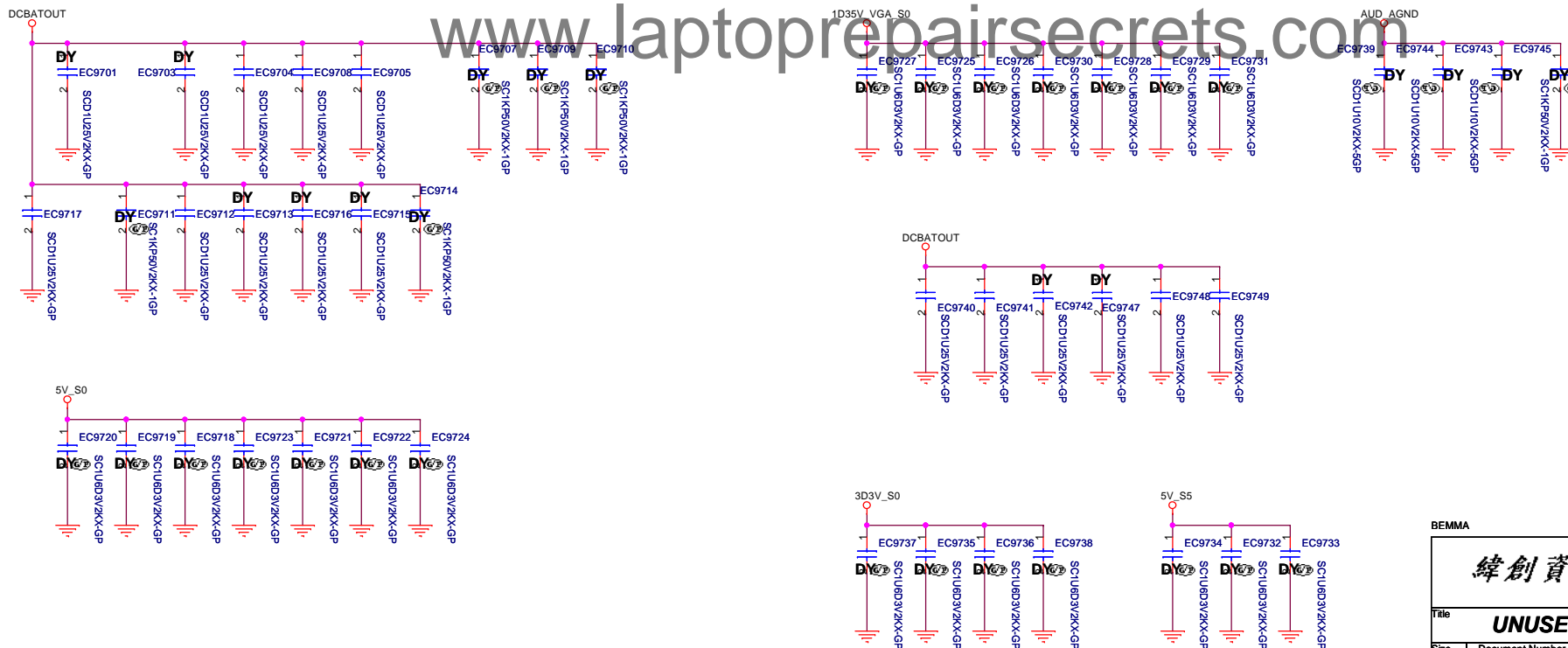
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Size <div>A4</div>	Document Number <div>Janus AMD BEEMA</div>	Rev <div>A00</div>
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## SSID = Mechanical



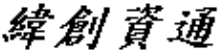
## SSID = EMI



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Title			
<b><i>NFC(Reserved)</i></b>			
Size A4	Document Number		Rev
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Title	
TEST PAD	
Size C	Document Number Janus AMD BEEMA
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Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Janus AMD BEEMA</div>	Rev <div>A00</div>
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Title <div>(Reserved)</div>		
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Title <div>(Reserved)</div>	
Size <div>A4</div>	Document Number <div>Janus AMD BEEMA</div>
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Title <div>(Reserved)</div>		
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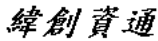
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Title			
<b>MCP CPU XDP HDT+</b>			
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Title		
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緯創資通

Wistron Corporation

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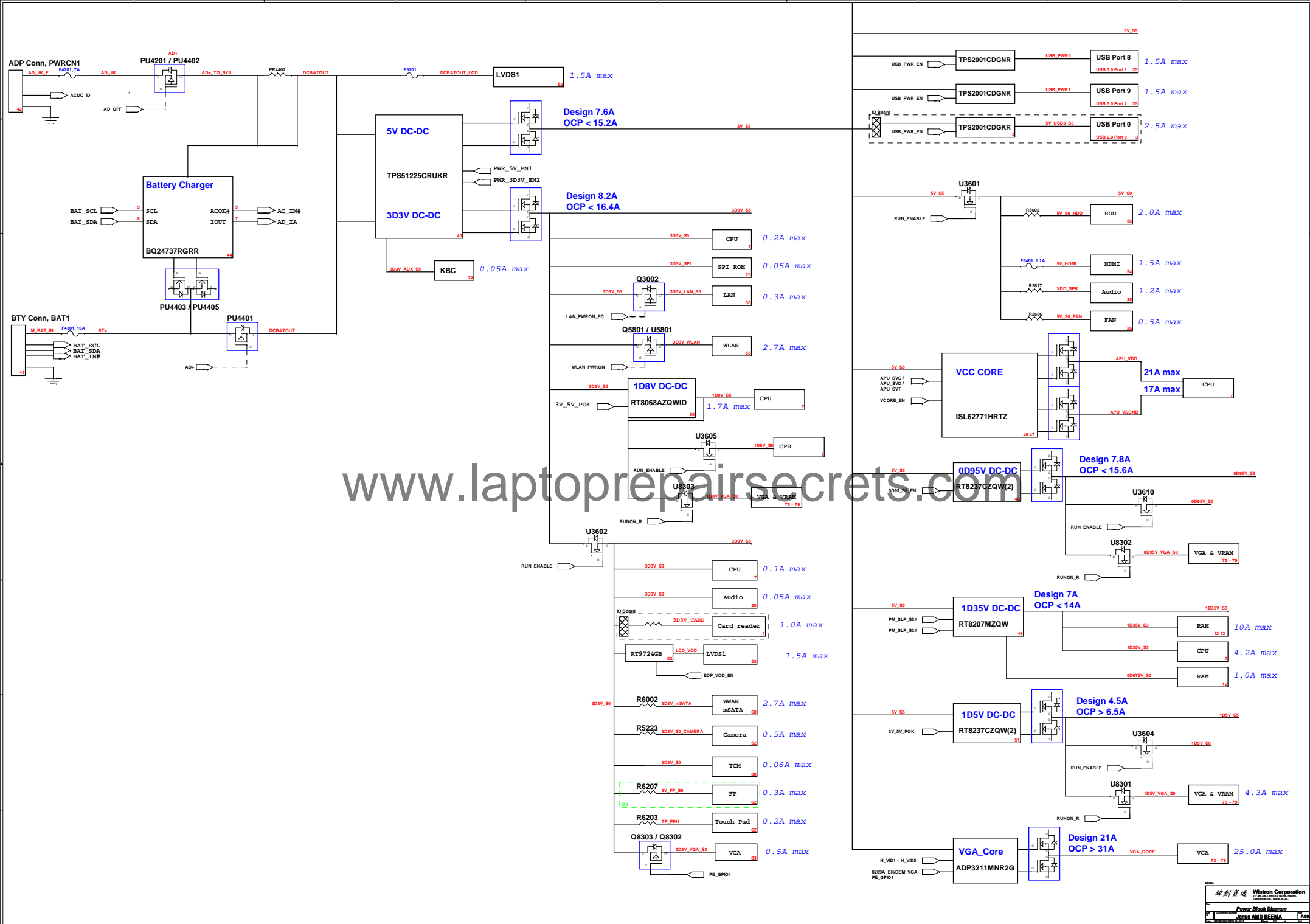
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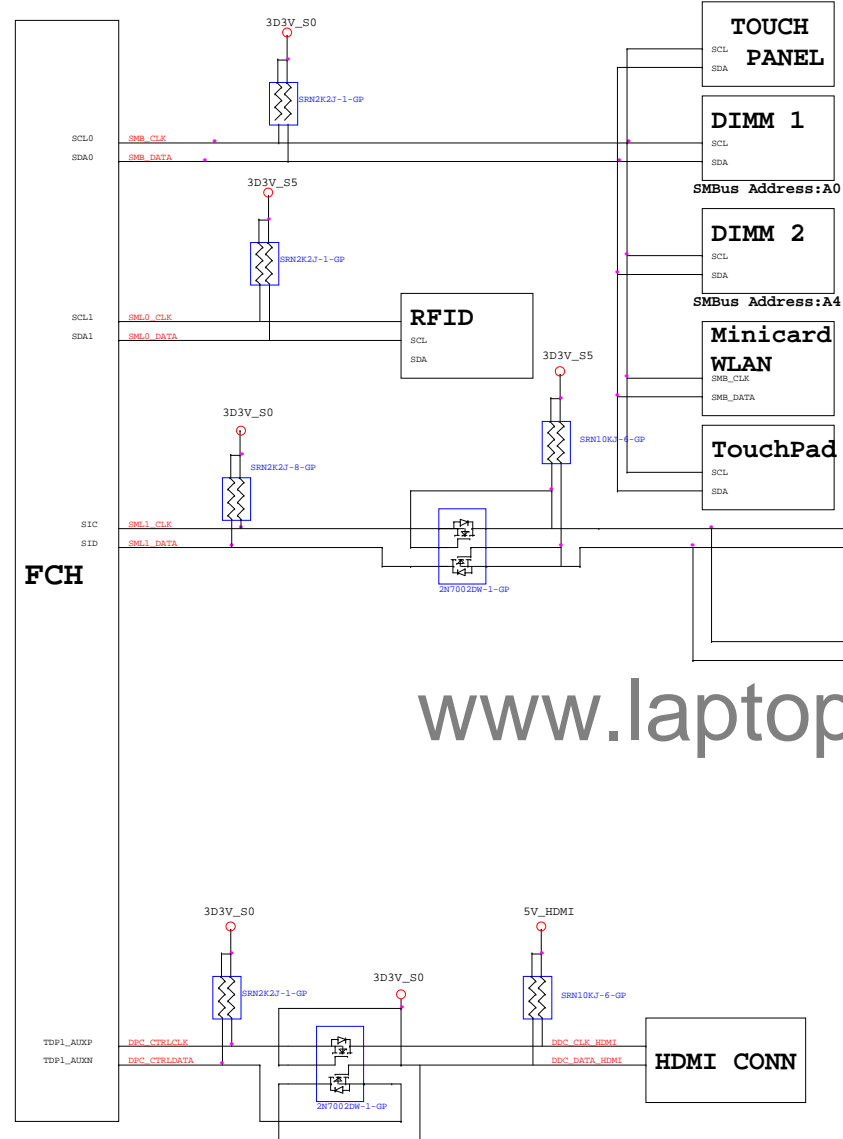
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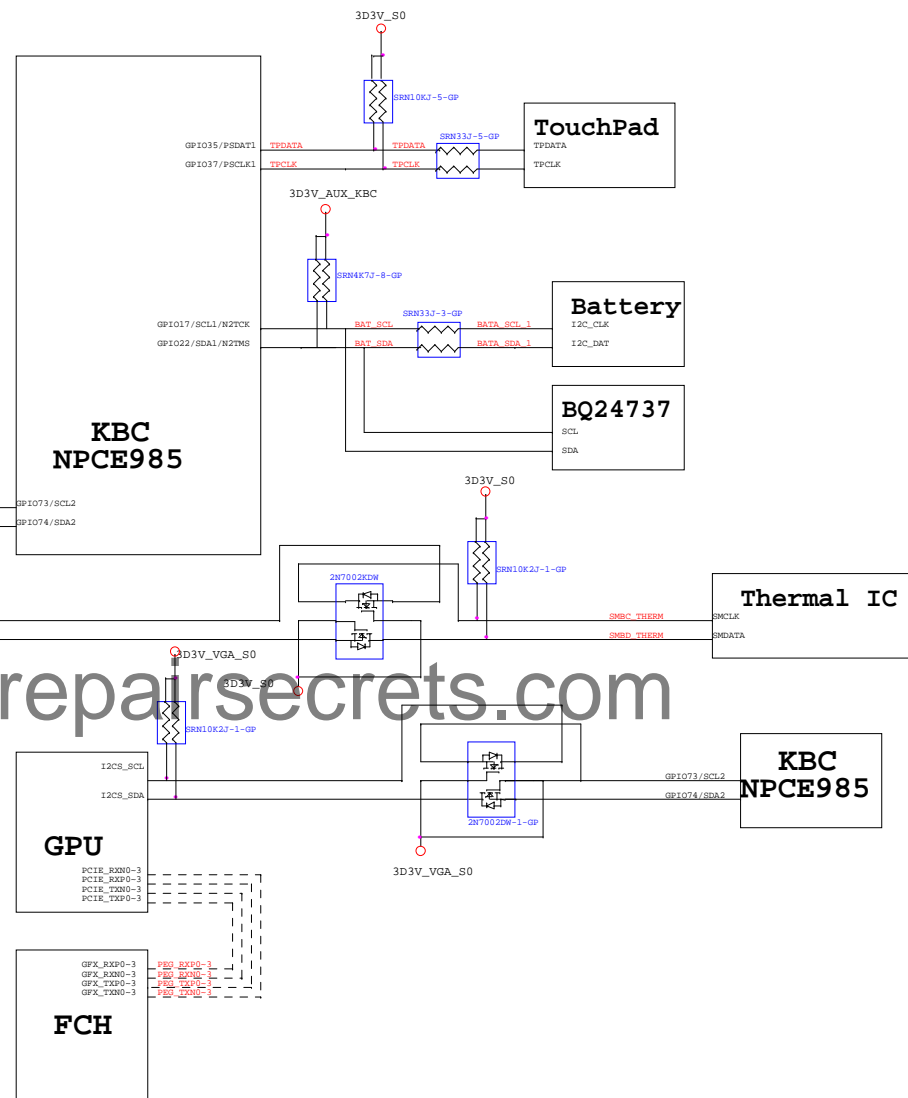
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# PCH SMBus Block Diagram

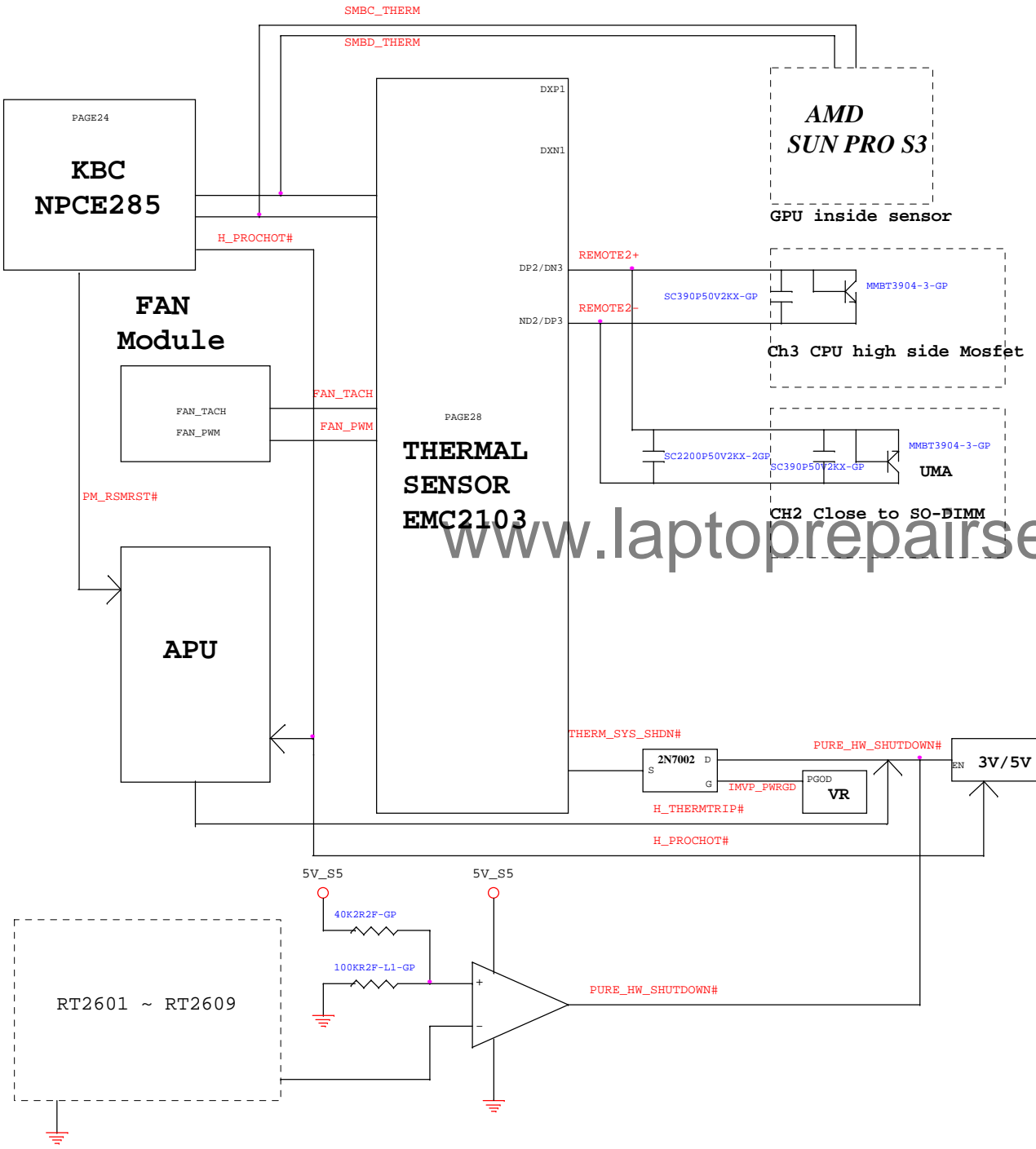


# KBC SMBus Block Diagram

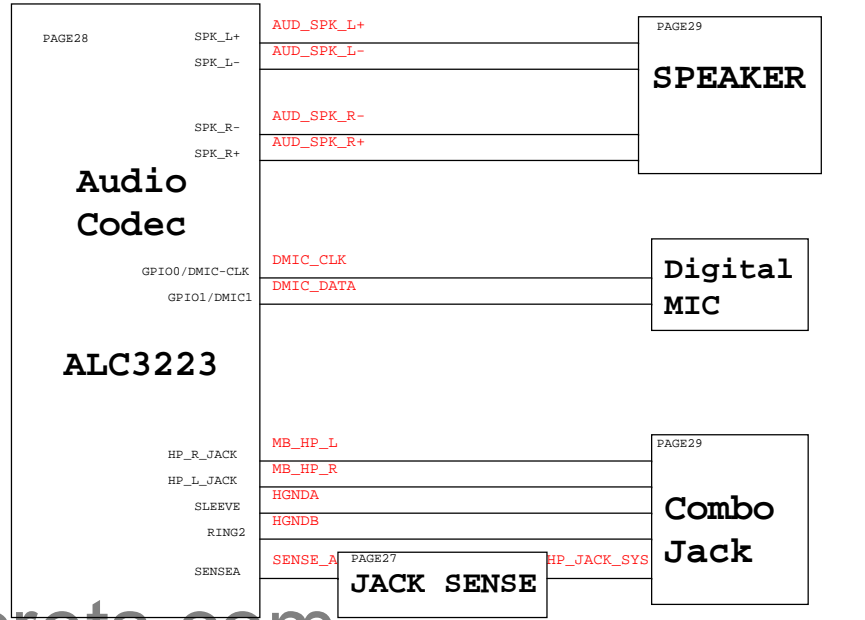


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Thermal Block Diagram



Audio Block Diagram



## Change notes -

	VERSION	DATE	Page	Modify List	OWNER
	X01	2013/12/3	83	R8309 = 15Kohm ,C8301/C8313 = DY,C8302 = 1000pF	
	X01	2013/12/3	43 44	RN4301 to 100ohm, AC_IN# change to Pull-H 3D3V_AUX_S5(PR4434)	
	X01	2013/12/3	27	HDA27 change from ALS3223 to ALC3234	
	X01	2013/12/3	24 25	Swap BATT_WHITE_LED# and EC_BRIGHTNESS. BATT_WHITE_LED# to GPIO13 and EC_BRIGHTNESS to GPIO15. Change R2404 from 10K to 20K ohm for PCB VERSION strap , Del SKT25	
	X01	2013/12/3	52	Reserve 0805 0 ohm R5211 between LCDVDD and LCD1.F5201 change from 69.50007.A31 to 69.60040.001	
	X01	2013/12/3	Power	Change C5205,EC4304,EC4601,PC4409,PC4419,PC4511.PC4518,PC4524,PC4720,PC4722,PC4827,PC4913 to 78.10422.2BL (0.1U 25V K0603 X7R) from 78.10424.2BL (0.1U 50V K0603 X7R).	
	X01	2013/12/3	54 55	Add HDMI SMBUS use 0 ohm DUMMY co-lay ,Add Hsync Vsync 0ohm DUMMY co-lay	
	X01	2013/12/3	29	Change HPMIC1 to 022.10002.0001 from 22.10270.G61 SPK1 change to 20.F1639.004	
	X01	2013/12/3	34 63	Change USB1 to 22.10341.Q21 / Change KBLIT1 to 20.K0800.004	
	X01	2013/12/3	19 26	Change C1904 and C1905 from 10pf to 6.8pf / Q2601 RN2602 DUMMY, RN2601 install	
	X01	2013/12/3	30	R3004 CLK_LAN_REQ0#_R change pull high to 3D3V_S0	
	X01	2013/12/3	EMI	DMIC_CLK mount R2716 100ohm resistance,Mount EC9749,Mount EC4304	
	X01	2013/12/3	58	CARD_WLAN_OUT# and CARD_WPAN_OUT# modify to TP change WLAN1 to 62.10043.I81	
	X01	2013/12/3	42 51	DCIN1 change to 20.F1783.007,Del 1D5V_S5 circuit	
	X01	2013/12/4	24 34 35	R2447 change to 63.10334.1DL,Del U3502 and U3501,swap the net U3403.1 and U3403.3	
	X01	2013/12/5	42 46 24 26	Del AFTP3804 AFTP3807, Modify AFTP6241 Add AFTP6242,Change R2447 to 1K , R2622 change to 24.3K	
	X01	2013/12/6	24	R2411 DY D2401 install	
	X01	2013/12/9	31 47 82	RJ45 connector change to 022.10001.0551, PT4701 /PT4704/PT8204 change to 79.3371V.6CL	
	X01	2013/12/10	EMI	Mount EC4303 and change to 0.1u Mount EC9705 EC9748 EC9717 EC9740 EC9741 EC9712 EC9704 EC9708 and change to 0.1u Mount R5415、R5417、R5416、R5414 150ohm resistance Mount TR3401、TR3404、TR6301(69.10103.041、69.10080.011) Mount TR5208、TR5209(69.10103.041、69.10080.011) Mount EC2705、EC2703、EC9739、EC9743、EC9744 0.1u cap Mount SPR2、SPR5、SPR6	
	X01	2013/12/10	0 ohm	change 0 ohm to short pad	
	X01	2013/12/10	54 55	R5501/R5502 change to 33 ohm / Del D5402	
	X01	2013/12/10	24 52 62	R2411 Install D2401 DUMMY ,R5207 BOM control ,BOM control DVC50 to Janus	
	X01	2013/12/12	46 86 62	PR4609 change to 44.2K (64.44225.6DL) from short pad, EMI:Add SPR6(34.42T14.002),KBLIT DUMMY	
	X01	2013/12/16	55 Power	Del HDMI circuit / Modify power schematic BOM	
	X01	2013/12/18	Power	PR8214 change to 499K (64.49935.6DL) / PR8215 change to 9.76K (64.97615.6DL)	

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	VERSION	DATE	Page	Modify List	OWNER
	X02	2014/01/21	48	Change PR4823 to 26.1K. The voltage about 0.97V	
	X02	2014/01/21	83	R8310 change 15Kohm /C8313 change 0.1uF /C8301 change 470pF Add R8301 for power sequence	
	X02	2014/01/27	12,46	EMC request:change EC4601,C1217,C1225,C1214 to 0.1u	
	X02	2014/01/27		Change 0 ohm to short pad	
	X02	2014/01/27	6	DGPU_PRESENT# pull hi to 3D3V_S0	
	X02	2014/01/28	power	1. PD4201 change 1st source to 83.P6SBM.AAG and 2nd source to 83.P6SBM.DAG . 2. PC4202 PC4409 PC4419 PC4519 PC4524 PC4511 PC4513 PC4518 PC4734 PC4720 PC4722 PC4736 PC4833 PC4827 PC4919 PC4913 PC8230 change to 78.10424.2BL. 3. PC4201 change to 78.10594.41L. 4. PC4916,PC4917 change to 78.10610.5BL. 5. PC4408 change to 78.47522.51L (4.7U 25V K0805 X5R). 6. PC4425 change to 78.10324.2FL (0.01U 50V K0402 X7R). 7. PC4512 change to 78.47522.51L (4.7U 25V K0805 X5R). 8. Delete PC4814/PC4714. 9. Dummy PC4718/PC4912/PC4920/PC4204/PC4205/ PC4426/PC4416/PC4830 10.PC4828 change to 78.47522.51L (4.7U 25V K0805 X5R). 11.PC4909 and PC4911 change to 78.47522.51L (4.7U 25V K0805 X5R).	
	X02	2014/02/06	06 19	Change RN1901 R1901 from short pad to 0 ohm Change RN604 to 66.10336.08L	
	X02	2014/02/06	86	Change SPR4 P/N to 34.15J03.001	
	X02	2014/02/07	26	THM26 DUMMY, Add R2602 for VD_OUT1# connect PURE_HW_SHUTDOWN#	
	A00	2014/02/25		Change PR4911 PR4649 R3016 R6209 R1901 RN5404 RN1901 to short pad	
	A00	2014/02/25	82	Modify schematic PWR_VGA_COMP connecte to PWR_VGA_FB	
	A00	2014/02/25	24	PCB VERSION A/D(PIN98) R2404 change to 64.64925.6DL	